The Dissertation Committee for Yeon Taek Jeong Certifies that this is the approved version of the following dissertation:

Analyses of Device Characteristics in Low Voltage *p*-, New Material *n*-, and Dual-channel Organic Field-Effect Transistors

Committee:

Ananth Dodabalapur, Supervisor

Paul S. Ho

Dean P. Neikirk

Jack C. Lee

Brian A. Korgel

Analyses of Device Characteristics in Low Voltage *p*-, New Material *n*-, and Dual-channel Organic Field-Effect Transistors

by

Yeon Taek Jeong, B.S.; M.S.E.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

May, 2008

Dedication

To my dearest mother Seong Soon Lee and father Jeong Hwa Jeong:

Acknowledgements

First of all, I would like to thank Dr. Ananth Dodabalapur for his supervision and help throughout the whole period of my research and dissertation activities. I also have to express my gratitude to Dr. Paul S. Ho, Dr. Dean P. Neikirk, Dr. Jack C. Lee, and Dr Brain A. Korgel for serving as my dissertation committee. The endless love from all my family and the financial support from Samsung Electronics, Inc. played an indispensible role in completing my Ph.D. work. Moreover, I am very grateful for the helpful discussions and advice from my former and current group colleagues: Dr. Liang Wang, Dr. Tae-ho Jung, Dr. Byungwook Yoo, Dr. Daniel H. Fine, Dr. Debarshi Basu, Dr. Suvid Nadkarni, Deepak Sharma, Cynthia F. Burham, Jacopo Testa, and Sebastian P. Schoefer; Dr. Soumya Dutta, Larry Dunn, Christopher J. Lombardo, Davianne A. Duarte, Shannon D. Lewis, Brian H. Cobb, Jae Won Shim, Dharmendar R. Palle, Chen-Guan Lee, and Saranjit Kaur. I also have to express deep thanks to Dr. Tobin J. Marks, Dr. Antonio Facchetti, and Dr. Michael R. Wasieleski at Northwestern University for supplying PDI-8CN_2. Special tributes are paid to Dr. Kenneth M. Ralls and Dr. John B. Goodenough. Dr. Ralls inspired me to set guidelines for how to live in the U.S. One low grade by Dr. Goodenough has kept me alert throughout the remaining classes. Finally, I have to say that this dissertation could not be completed without the invaluable English corrections by Ms. Heather Schulman.

Analyses of Device characteristics in Low Voltage *p*-, New Material *n*-, and Dual-channel Organic Field-Effect Transistors

Publication No._____

Yeon Taek Jeong, Ph.D.

The University of Texas at Austin, 2008

Supervisor: Ananth Dodabalapur

This dissertation consists of three main chapters: Pentacene-based low voltage *p*-channel organic filed-effect transistors (OFETs) with anodized gate dielectrics; Charge transport in *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) [PDI-8CN_2] based *n*-channel OFETs; and Dual-channel OFETs. Pentacene-based low voltage *p*-channel OFETs were realized using three different anodized gate dielectrics: a 470 Å SiO_2, a 1,700 Å Ta_2O_5, and an 800 Å Ta_2O_5 formed by anodizing an *n*-Si wafer, a sputtered Ta thin film, and an e-beam evaporated Ta layer, respectively. Devices with the anodized SiO_2 gate dielectric exhibited decent characteristics at $V_{DS} \leq$ -10 V and $V_G \leq$ -4 V, and the device performance was further improved by an octyltrichlorosilane (OTS) treatment. The two anodized Ta_2O_5 gate dielectrics were successfully employed to fabricate devices with high mobility at $V_{DS} \leq$ -5 V and $V_G \leq$ -2.5 V for the 1,700 Å Ta_2O_5 devices, and at $V_{DS} \leq$ -10 V and $V_G \leq$ -5 V for the 800 Å Ta_2O_5 devices. A hexamethyldisilazane (HMDS) treatment and a mono-docecyl phosphate (MDP) treatment proved to remarkably enhance the characteristics of the two Ta_2O_5 devices.

However, the two treatments had the opposite influence on the threshold voltages of the devices from each other because of the capacitance difference resulting from their molecular length difference. In order to establish the suitable charge transport mechanisms in PDI-8CN_2 and related *n*-channel organic semiconductors, the gate voltage and temperature dependence of electrical behavior and the contact resistance effects were studied in PDI-8CN_2 based OFETs. The dependence of electrical behavior such as mobility, field-dependent mobility, trap density, and off current on gate voltage and temperature was derived using the multiple trapping and release (MTR) model. The contact resistance effects were determined by calculating the contact-corrected linear regime mobility and contact resistance by means of a four-probe measurement technique. Organic dual-channel OFETs were realized using poly-3-hexylthiophene (P3HT), PDI-8CN_2, and a polymeric dielectric (Merck® DS121) as the *p*-channel, *n*-channel, and gate dielectric materials, respectively. Coupled with each other, the *p*-FET and the *n*-FET showed acceptable characteristics at $|V_{DS}| \leq 50$ V and $|V_G| \leq 50$ V. Both the *p*-FET mode and the *n*-FET mode responded to delivered IPA and ethanol vapors with reasonably high sensitivity, which suggests that these organic dual-channel devices are effectively applicable to organic chemical sensing.

Table of Contents

List of Tables

List of Figures

CHAPTER 1 INTRODUCTION

1.1 Organic semiconductors

1.1.1 Small Molecule Organic Semiconductors & Conducting Polymers

Organic semiconductors have been studied since the late 1940s and are attracting increased attention because of their potential applications to thin-film transistors [1-3], light-emitting diodes [4-6], photovoltaic cells [7-9], photoexcited lasers [10,11], etc. There are two main categories of organic semiconductors: small molecule organic semiconductors and π-conjugated polymers. Since the first demonstration of organic thin-film transistors using copper-phthalocyanine (CuPc) in 1964, there has been remarkable progress in small molecule organic semiconductor devices [1]. Meanwhile, conducting polymers, which were first discovered by Alan J. Heeger *et al.* in 1976, proved to be able to exhibit even metal-like conductivity by various doping methods [12-14]. In terms of device characteristics, there have been numerous reports on the improved characteristics of organic field-effect transistors (OFETs), with demonstrated higher mobilities than those of typical inorganic *a*-Si:H counterparts [1].

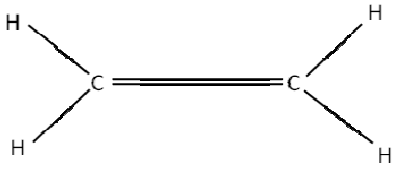
1.1.2 Charge Transport in Organic Semiconductors

In crystalline inorganic semiconductors such as Si or GaAs, two sets of energy bands are formed by the interaction between atoms when they are brought together. The completely electron-filled "valence band" is separated from the empty "conduction band" by a forbidden energy gap [15]. In organic semiconductors, however, the band formation

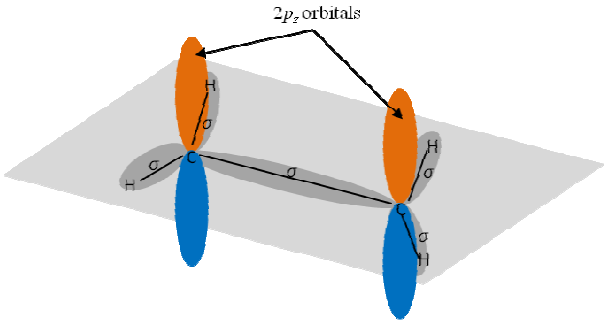
is explicable by the overlapping of p_z orbitals of carbon atoms. The one 2*s* atomic orbital and the two 2*p* atomic orbitals ($2p_x$, $2p_y$) in a carbon atom generate three equivalent planar-trigonal orbitals: sp^2 hybridization. These three hybridized orbitals form three σ-bonds with two adjacent H atoms and a C atom. However, the third $2p_z$ orbital is not involved in the hybridization and stays perpendicular to the plane of the three sp^2 hybrid orbitals. The remaining $2p_z$ orbitals on neighboring carbon atoms lie parallel to each other and overlap to form a π-bond, which establishes a delocalized electron density (Fig. 1.1) [16]. The alternative single and double bonds enable a delocalized electron to migrate through organic molecules or conjugate polymers, from which their semiconducting properties result.

In organic semiconductors, the splitting of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) result from the interaction between adjacent molecules or chains. Fig. 1.2 illustrates the bonding-antibonding interaction between the HOMO/LUMO levels of two ethylene (C_2H_4) molecules [17]. Considering that a $2p_z$ orbital consists of two lobes centered about the nodal plane, the ethylene molecule will be in a minimum energy-state with the adjacent lobes of same wave function. When the two molecules are brought together, an energy splitting occurs depending on the way they combine with each other. If a large number of interacting molecules along with their energy splitting are taken into consideration, the energy splitting forms an energy band which is occupied by electrons: the valence band (HOMO). In contrast, the ethylene molecule is under a maximum energy-state if the neighboring lobes have different wave function from each other. The combination of the

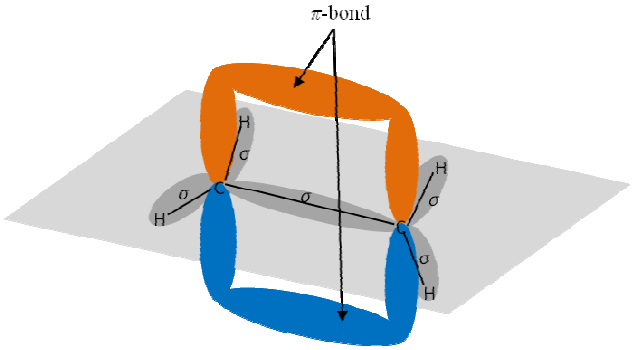
molecules gives rise to an energy splitting, whose level is higher than the case of the minimum energy-state. With the consideration of a large number of those interacting molecules with their energy splitting, the electron-free conduction band (LUMO) is formed. The splitting of the HOMO and the LUMO produces the transfer integral *t* that expresses the ease of transfer of a charge (electron/hole) between two interacting molecules or chains. The bandwidth *W* is related to the transfer integral by $t = h/2\pi\, W$, where h is Planck's constant (h = 4.14 $\times 10^{-15}$ eV-s). Therefore, the larger the HOMO bandwidth, the higher the hole mobility; the larger LUMO bandwidth, the higher the electron mobility.



(a) Lewis structure of a C_2H_4 molecule



(b) σ-bond formation in a C_2H_4 molecule



(c) π-bond formation in a C_2H_4 molecule

Fig. 1.1 Bond formations in an ethylene (C_2H_4) molecule: (a) Lewis structure of C_2H_4, (b) σ-bond formation, and (c) π-bond formation. Three hybridized sp^2 orbitals form three σ-bonds with two adjacent H atoms and a C atom. The remaining $2p_z$ orbitals on neighboring carbon atoms lie parallel to each other and overlap to form a π-bond, which establishes a delocalized electron density [From 16].

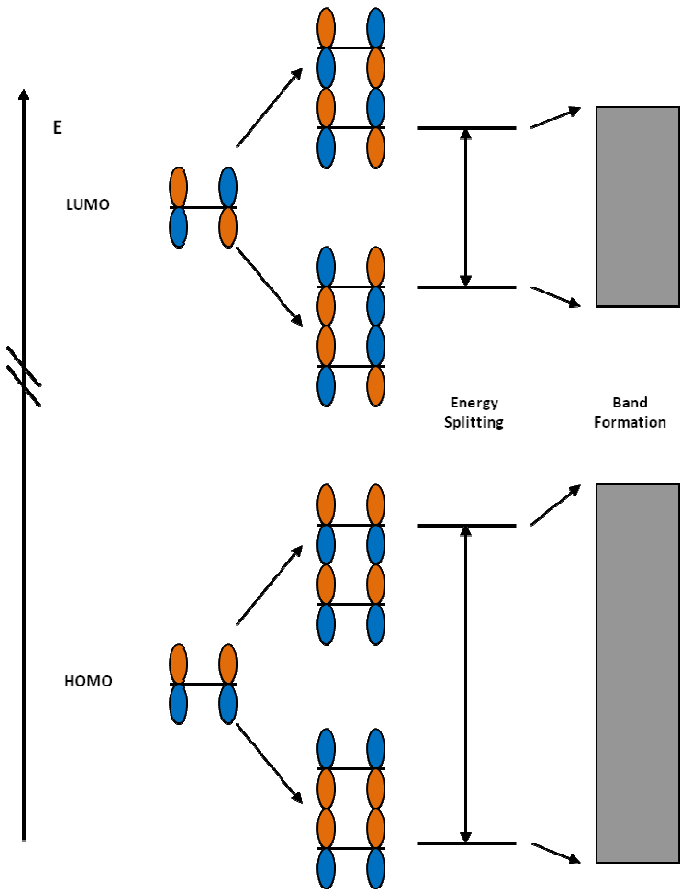


Fig 1.2 Illustration of band formations in organic semiconductors using ethylene (C_2H_4) as an example: The ethylene molecule will be in a minimum energy-state with the adjacent lobes of same wave function. When the two molecules are brought together, an energy splitting occurs depending on the way they combine with each other. If a large number of interacting molecules along with their energy splitting are taken into consideration, the energy splitting forms an energy band which is occupied by electrons: the valence band (HOMO). In contrast, if the neighboring lobes have different wave function from each other, the combination of the molecules gives rise to an energy splitting, whose level is higher than the case of the minimum energy-state. With the consideration of a large number of those interacting molecules with their energy splitting, the electron-free conduction band (LUMO) is formed [From 17].

The charge transport mechanism in crystalline organic or highly ordered semiconductors is temperature-dependent. At low temperatures, band-like transport can exist when disorder is minimal and the widths of the bands are sufficiently large, as is the case with typical inorganic semiconductors like Si. In order for band transport to occur, however, other certain criteria need to be met other than ordering and π-orbital overlapping. These criteria include the following:

1. The bandwidth W must be greater than kT: $W > kT$.
2. The mean free path of a carrier has to be greater than the inter-molecular spacing.
3. The bandwidth W should be greater than the dominant phonon energy $h\omega$ in a system: $W > h\omega$.

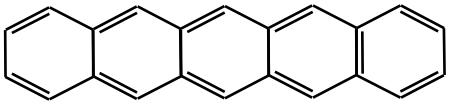
With a few approximations and assumptions, it turns out that the carrier mobility value of 1 $cm^2/V.s$ is a very good estimate for the existence of band transport. In other words, if the mobility is greater than 1 $cm^2/V.s$ under a certain circumstance, band-like charge transport can take place. However, as temperature increases, the effective bandwidths are gradually reduced by phonon-scattering processes [17]. Interestingly enough, typical organic semiconductors have strong electron-phonon coupling, which results in a rather steep temperature dependence of electronic bandwidth. With the electron-phonon coupling constant on the order of one or more, the bandwidth tends to decrease very sharply as temperature increases. The net effect is steeply reduced mobility with the increase in temperature and an early onset in the band to hopping transition; the charge carriers become localized over single molecules or chains and the charge transport

is governed by a thermally activated hopping mechanism [18]. According to semi-classical electron transfer theory, the hopping rate (k_{ET}) can be approximately expressed by [19,20]

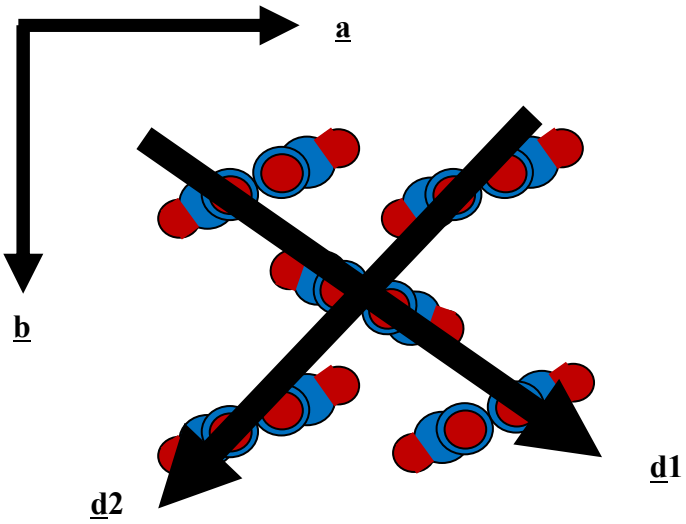
$$k_{ET} = \frac{4\pi^2}{h}\frac{1}{\sqrt{4\pi kT}}t^2 \exp\left(-\frac{\lambda}{4kT}\right) \tag{1.1}$$

where T is temperature, λ is reorganization energy, t is transfer integral, h is Planck's constant, and k is Boltzmann constant. Equation (1.1) implies that fast charge transfer processes within a hopping regime require large transfer integrals and a weak electron-phonon coupling.

A lot of organic molecular crystals pack in what is called herringbone structure, which produces the closest packing of the molecules. For example, pentacene molecules stack to form a herringbone pattern that results in highly dense packing with a larger overlap of molecular orbitals (Fig. 1.3) [21,22]. Total splitting is calculated along axis d2 and d1 as well as axis a and axis b. The π-orbital overlapping is higher along these axes; the charges can transfer from one molecule to another with relative ease. Interlayer splitting along aixs c perpendicular to the paper plane, however, is almost negligible. Because there is a lesser degree of π-orbital overlapping along this direction, the charges will undergo difficulty in moving from one layer to another. As a result, the transport in molecules with herringbone packing is anisotropic; charge transport depends on the degree of ordering of molecules or chains as well as the density of chemical/structural defects.



(a) Molecular structure of pentacene



(b) Herringbone-packed pentacene molecules

Fig. 1.3 Herringbone packing of pentacene molecules: Total splitting is calculated along axis d2 and d1 as well as axis a and axis b. The π-orbital overlapping is higher along these axes; the charges can transfer from one molecule to another with relative ease. Interlayer splitting along aixs c perpendicular to the paper plane, however, is almost negligible. Because there is a lesser degree of π-orbital overlapping along this direction, the charges will undergo difficulty in moving from one layer to another.

1.2 Organic Field-Effect Transistors

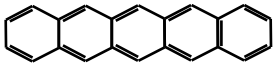
1.2.1 Hole transporting & Electron transporting Organic Semiconductors

In terms of charge carriers, just as in inorganic semiconductors, there are two types of organic semiconducting materials: *p*-type and *n*-type organic semiconductors, whose main carriers are holes and electrons, respectively. There has been remarkable progress in enhancing the properties and understanding characteristics of *p*-type organic semiconductors such as pentacene, copper phthalocyanine (CuPc), rubrene, and regio-regular poly (3-hexylthiophene) (P3HT). Such semiconductors transport holes more efficiently than electrons. In contrast, there are several reasons for the slow development in *n*-type organic semiconducting materials [23]:

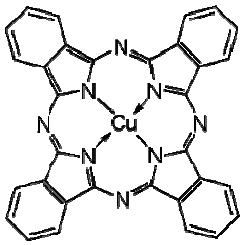
1. Electrons tend to be trapped in the presence of O_2 and H_2O.
2. Typical organic semiconductors have relatively small electron affinity. Therefore, electron-withdrawing side groups are required to stabilize the anionic forms of molecules and to efficiently transport electrons.
3. General contact metals such as Au or Ag have work function levels more favorable for the hole-injection than the electron-injection in typical organic semiconductors. The trials of using low work function metals were unsuccessful because of their oxidation and complex formation.

Nevertheless, there recently have been significant reports on synthesizing new *n*-type organic semiconductors, which are essential for realizing complementary circuits as well as forming efficient electron transporting layers in light emitting diodes (LEDs) or solar cells [23-26]. The prevalent way of synthesizing *n*-type organic semiconductors is

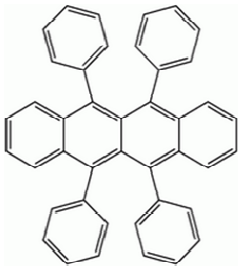
adding electron-withdrawing side groups such as cyano or perfluoroalkyl to *p*-type cores like naphthalene, perylene, or 6T. Presently, extensive work is being done on naphthalene and perylene cores with electron-withdrawing dianhydride or diimide moieties. The examples of *n*-type organic semiconductors include N,N'-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2); N-N fdioctyl-3,4,9,10-perylene tetracarboxylic diimide (PTCDI-C8); carbonyl-substituted (α,ω-diperfluorohexyl-4T) (DFHCO-4T); and copper hexadecafluorophthalocyanine (F_{16}CuPc). Fig.1.4 illustrates the molecular (polymeric) structures of several common *p*-type and *n*-type organic semiconductors.



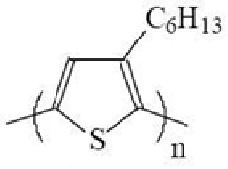
Pentacene



CuPc

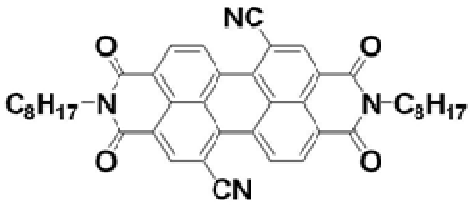


Rubrene

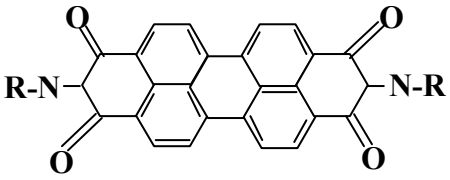


P3HT

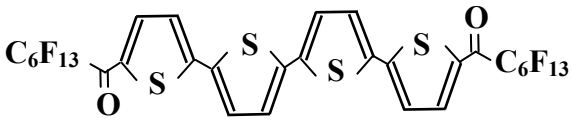
(a) *p*-type hole-transporting organic semiconductors



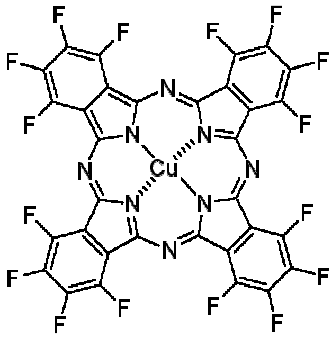
PDI-8CN$_2$



PTCDI-C8



DFHCO-4T



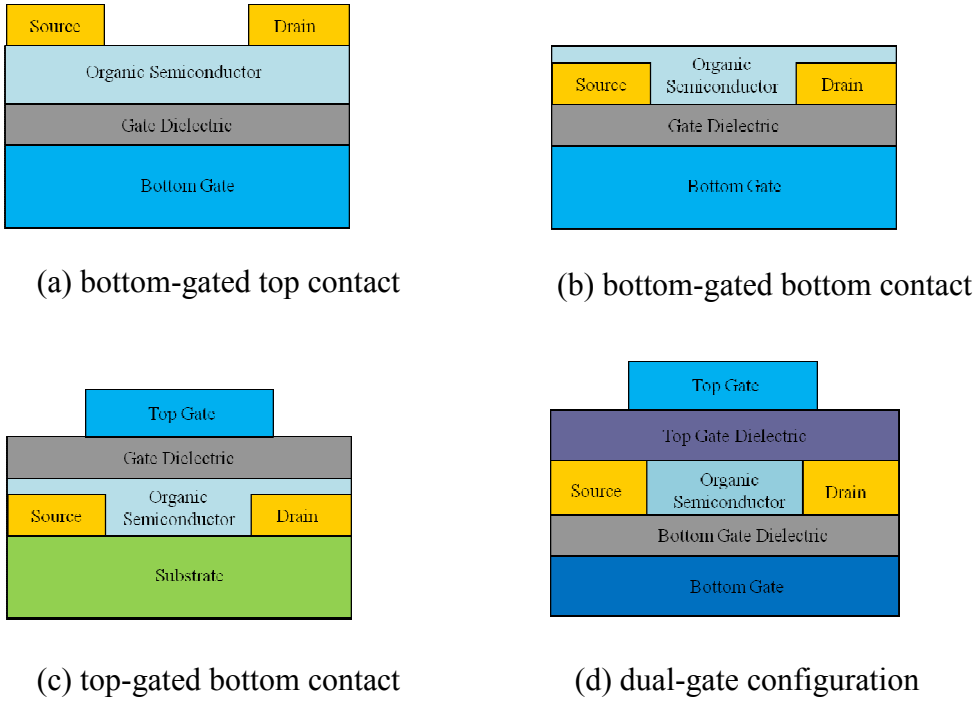
F$_{16}$CuPc

(b) *n*-type electron-transporting organic semiconductors

Fig. 1.4 Molecular structures of common organic semiconductors: (a) *p*-type hole-transporting organic semiconductors (b) *n*-type electron-transporting organic semiconductors.

1.2.2 *P*-, *N*-, AND DUAL-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS

In organic field-effect transistors (OFETs), the channel is formed by the accumulation of the main charge carriers of the organic semiconductor in question: a *p*-type material typically forms a *p*-channel, an *n*-type material forms an *n*-channel. However, it must be noted that with the use of some gate dielectrics, typically *p*-FET forming materials such as pentacene can exhibit *n*-channel behavior as well. By contrast, inorganic FETs are usually operated in inversion mode: *p*-channels and *n*-channels are formed with *n*-type and *p*-type substrates, respectively [27,28]. This is one of the main properties of OFETs that distinguish them from their inorganic counterparts.



(a) bottom-gated top contact

(b) bottom-gated bottom contact

(c) top-gated bottom contact

(d) dual-gate configuration

Fig. 1.5 Schematics of OFET configurations: (a) bottom-gated top contact, (b) bottom-gated bottom contact, (c) top-gated bottom contact, and (d) dual-gate configuration.

The structures of OFETs are divided into top-contact or bottom-contact configurations depending on the sequence in which the organic layer and the electrode layer are formed. For a top-contact configuration, an organic layer is deposited prior to an electrode layer. A bottom-contact configuration has the reverse deposition sequence. Meanwhile, an OFET is said to have bottom-gate or top-gate structure by the relative location of the gate electrode with respect to the gate dielectric. In a bottom-gate structure, the gate-electrode has a lower location relative to the gate dielectric; in contrast, the gate-electrode is located in the upper position in a top-gate device structure. A dual-gate structure is also viable, in which an OFET has top-gate and bottom-gate structures in a device configuration. Fig. 1.5 illustrates the schematic structures of OFETs discussed.

As is the case with inorganic metal-oxide-semiconductor field-effect transistors (MOSFETs), silicon dioxide (SiO_2) is widely used as the gate dielectric material to implement OFETs because it is chemically stable and exhibits reasonably low gate leakage current. However, in order to make the best use of the unique properties of organic semiconductors such as low temperature process and flexibility, polymeric dielectrics are getting more and more attention [29-32]. The realization of OFETs with low operating voltages is another current issue that earns much interest. There have been reports on using high-*k* gate dielectrics such as Al_2O_3 [33] and Ta_2O_5 [34,35] to achieve this goal. Self-assembled monolayer (SAM) dielectrics can also be considered as an alternative way to that end [36-39].

By far, gold (Au) is the most widely used metal for the source and drain electrodes in OFETs, whose decent work function of 5.1 eV is favorable to both hole and electron injection in common organic materials. However, the relatively hydrophilic nature of a Au surface tends to cause many organic semiconducting molecules to lie flat. In this case, the organic molecules are poorly ordered over the contact electrodes, thereby increasing the contact resistance at the electrode/semiconductor interface. The net effect is the degradation of device performance; the degradation becomes much more significant as the channel length is continuously scaled down, which is frequently observable in nano-scale OFETs. There are two generally suggested methods to solve the problem. One is employing SAM treatments to the noble metal electrodes such as Au, Ag, or Pd; the other is using conducting polymers like poly(3,4-ethylenedioxythiphene)/poly(styrene sulfonate) (PEDOT/PSS) as the substitute for metal electrodes. SAMs are ordered molecular assemblies formed by the adsorption of an active surfactant on a solid surface. A SAM treatment at the interface between metal/semiconductor results in improved properties by lowering surface energy differences, which facilitates the formation of ordered thin films [1,40]. It is well-known that alkanethiols form SAMs with excellent properties on noble metals [1,41-45]. Among conducting polymers, water-soluble PEDOT/PSS has a few salient properties that make it suitable for the electrode material replacing metals. These properties include low oxidation potential, moderate bandgap of 1.6 eV, good film formation, high visible light transmission, and high stability. Because solution-based PEDOT/PSS can be processed

by spin-coating or ink-jet printing techniques, it has been widely studied for applications to organic LEDs, organic photovoltaic cells, and OTFTs [46-50].

Organic semiconductors are deposited by high-vacuum sublimation or solution-casting process [1]. A lot of small molecule organic semiconductors are deposited by vacuum sublimation. However, vacuum sublimation has a major drawback to practical applications in that fabrication cost becomes considerably high because of the requirement for high-vacuum equipment. Solution-based processing is thought of as a solution to the problem; in addition, this family of techniques also shows a lot of promise in large area applications and mass production in organic electronics. However, solution-based processing produces organic layers with relatively poor molecular ordering compared to vacuum sublimation. The problem of poor molecular ordering can be reduced by a suitable surface treatment on the surface of the gate dielectric of interest. In general, surface treatments are also effective in improving molecular ordering in vacuum-sublimated organic thin films.

The basic concept of surface treatment is to lower the surface energy of the gate dielectric by employing a SAM agent, thereby making its surface more hydrophobic [51]. To that end, organosilane SAMs have frequently been used. Hexamethyldisilazane (HMDS) is well-known for reducing the interaction between the organic molecules and the inorganic gate dielectrics like SiO_2 [52]. Some trichlorosilanes also prove to be effective in functionalizing the surface of the gate dielectrics; those trichlorosilanes include octadecyltrichlorosilane (OTS), 7-octenyltrichlorosialne (VTS), benzyltrichlorosilane (BTS), etc. [53,54].

As for the dimensionality of charge transport in OFETs, it has been shown that the field-induced conductivity is confined to the interfacial region of the organic semiconductor near the gate dielectric. In other words, the charge conduction in OFETs only occurs near the interfacial plane between the organic semiconductor layer and the gate dielectric [55]. Therefore, we can use the commonly-known 2-dimensional channel approximation in expressing the drain current of OFETs [15,27]. For low drain voltage (linear region) $|V_{DS}| < |V_G - V_T|$, the drain current I_D is given by

$$I_D = \frac{W\mu_{lin.}C_i}{L} \times \left((V_G - V_T)V_{DS} - \frac{{V_{DS}}^2}{2} \right) \tag{1.2}$$

where W, L, C_i, V_G, and V_T represent the channel width, the channel length, the capacitance of the gate dielectric per unit area, the gate voltage, and the threshold voltage, respectively. In the linear region, the drain current I_D increases linearly with the applied drain voltage. The linear region mobility $\mu_{lin.}$ can be calculated from the experimentally obtained transconductance $\partial I_D/\partial V_G$

$$\mu_{lin.} = \left(\frac{\partial I_D}{\partial V_G} \right)_{V_{DS}} \frac{L}{V_{DS}WC_i} \tag{1.3}$$

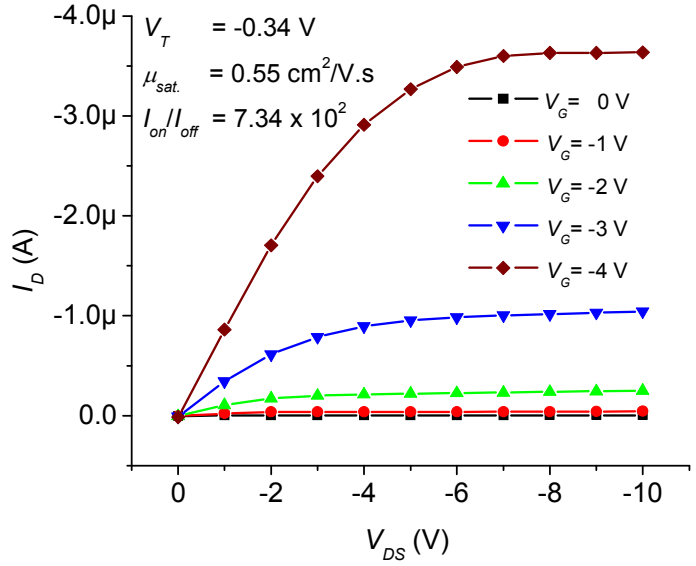
If drain voltage is large enough for $|V_{DS}| \geq |V_G - V_T|$, the device is in the saturation region with the saturation drain current I_{DS} given by

$$I_{DS} = \frac{W\mu_{sat.}C_i}{2L} \times (V_G - V_T)^2 \tag{1.4}$$

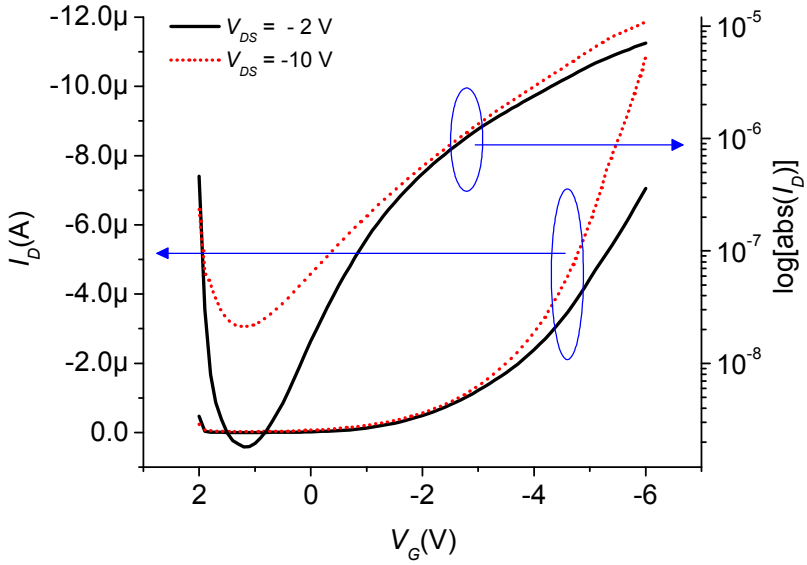
In the saturation region, the drain current remains essentially constant for drain voltage over $V_{DS,sat.} = V_G - V_T$. The saturation mobility $\mu_{sat.}$ is calculated from the slope of $\sqrt{|I_{DS}|}$ vs. V_G that is obtained from the output characteristics in the saturation region:

$$\mu_{sat.} = \left(\frac{\sqrt{|I_{DS}|}}{V_G} \right)^2_{V_{DS}} \frac{2L}{WC_i} \tag{1.5}$$

Fig. 1.6 presents (a) the output characteristics and (b) the transfer characteristics of a pentacene-based top-contact *p*-channel OFET, whose gate dielectric is made up of 470 Å SiO_2. Depending on the output characteristics of the device, the value of saturation mobility, threshold voltage, and I_{on}/I_{off} ratio are calculated to be 0.55 $cm^2/V.s$, -0.34 V, and 7.34×10^2, respectively.



(a) Output characteristics



(b) Transfer characteristics

Fig. 1.6 (a) Output characteristics and (b) transfer characteristics of a pentacene-based top-contact *p*-channel OFET, whose gate dielectric is made up of 470 Å SiO_2.

In general, *n*-channel OFETs have been less explored than their *p*-channel equivalents. This is due to their generally inferior characteristics to those of *p*-channel OFETs in the ambient environment. In other words, they mostly work well only under a high vacuum free of oxygen (O_2) or moisture (H_2O) [24,25,56]. It is thought that the problem comes from an extrinsic effect rather than the *n*-type semiconductor in itself [57,58]. An important reason is thought to be the trapping of electrons at the gate dielectric-semiconductor interface caused by electronegative hydroxyl (-OH) groups in the dielectric material. No electron trapping was observed when a hydroxyl-free material was used as gate dielectric in nitrogen. Accordingly, it is expected that *n*-channel OFETs can exhibit performance comparable to *p*-channel devices with the choice of suitable gate dielectric materials or surface treatment [58]. Additionally, the use of materials with suitably designed physical and chemical properties such as the LUMO level, e.g., PDI-$8CN_2$, will permit relatively stable operation in the ambient environment. Until now, there have been continuous reports on *n*-channel OFETs with their improved electron mobility [26,56,59-61].

Dual-channel OFETs are of much interest to those who work on organic chemical sensing. Basically, these devices are four-terminal OFETs that consist of a *p*-cannel and an *n*-channel coupled with each other. These organic dual-channel devices are promising because of their possible applications to chemically sensitive organic vapor sensing.

CHAPTER 2 PENTACENE-BASED LOW VOLTAGE *P*-CHANNEL OFETS WITH ANODIZED GATE DIELECTRICS

2.1 Introduction

Organic field-effect transistors (OFETs) have been attracting considerable attention because of their potential applications in active matrix display drivers, radio frequency identification tags, smart cards, sensor arrays, etc. [1,62-67]. Although there have been significant advances in fabricating OFETs with reasonably high electron and hole mobility [26], their generally high operating voltages still need to be reduced for many practical applications. Up to now, there have been several reports on realizing OFETs with low operating voltages. Some groups have proposed the use of high-*k* gate dielectrics such as Al_2O_3 [33] and Ta_2O_5 [34,35]. Self-assembled monolayer (SAM) dielectrics are yet another approach [36-39]. The use of Ta_2O_5 gate dialectic is quite attractive because of its high dielectric constant [68]. There are several different ways of forming a layer of Ta_2O_5 gate dielectric [34,35,69-71].

Anodic oxidation is a unique way of obtaining a Ta_2O_5 layer in that the process can be performed under the ambient environment with simple equipment [34,35,72]. Even though anodized Ta_2O_5 gate dielectrics exhibit relatively high gate leakage currents, the leakage currents are known to be greatly reduced by suitable surface treatments [73]. The surface treatments are also effective in ordering organic molecules, improving the mobility of OFETs by significant amounts.

Thermally grown SiO_2 is the most widely employed material as the gate dielectric in realizing initial test OFETs because of its desirable properties such as low leakage current, high breakdown voltage (10^7 V/cm), high chemical resistance with the exception of HF, moderate surface roughness (2.6 Å), etc. However, regardless of its inferior quality to thermally grown SiO_2, anodized SiO_2 is still usable as the gate dielectric in OFETs [35]. The problem of relatively high gate leakage of anodized SiO_2 is expected to decrease by suitable surface treatments.

This chapter covers the behavior of the pentacene-based low voltage *p*-channel OFETs with three different gate dielectrics: anodized SiO_2, anodized Ta_2O_5 obtained from a sputtered Ta layer, and anodized Ta_2O_5 obtained from an e-beam evaporated Ta thin film. The effects of three different surface treatments are also discussed: an octyltrichlorosilane (OTS) treatment on the anodized SiO_2 gate dielectric, a Hexamethyldisilazane (HMDS) treatment, and a mono-dodecyl phosphate (MDP) treatment on the two anodized Ta_2O_5 gate dielectrics.

2.2 Anodic oxidation

In an anodic oxidation, alternatively known as anodization, the anode (+) and the cathode (-) consist of a material electrode to be oxidized and a noble metal electrode, respectively. The anode and the cathode are immersed in an electrolyte and connected to an outer power supply (Fig. 2.1) [62].

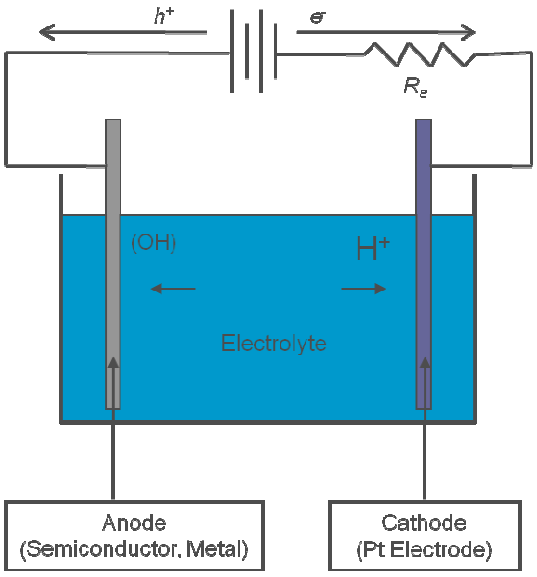


Fig. 2.1 Schematic of an anodization system, in which the anode (+, a material electrode to be oxidized) and the cathode (-, a noble metal electrode) are immersed in an electrolyte and connected to an outer power supply.

Depending on the source impedance R_s, anodization is performed in two different modes: a constant voltage mode for a very low R_s and a constant current mode for a very high R_s. Anode materials range from semiconductors such as Si or GaAs to metals such

as Al, Ta, or Ti. Platinum (Pt) is most widely used as the cathode. Even though various electrolytes are feasible, water (H_2O) is the most important oxidizing component for all electrolytes; H_2O dissociates into H^+ and $(OH)^-$. Usually, a small amount of a conductivity modifier is added to the electrolytes to change their resistance.

The consumed amount of an anodized material is predictable using Faraday's law of electrolysis. According to this law, the weight of a substance that undergoes the anodization is proportional to the quantity of electricity passed through the electrolyte [72,74]:

$$w = \frac{ItW}{F} \tag{2.1}$$

where w is the weight of reacted substance in grams, I is the current in amperes, and t is the time passed in seconds. W is the equivalent weight of the reacted substance in grams, which is equal to its atomic or molecular weight divided by the valence change in the anodization. F is the Faraday constant of 96,483 C/mol.

2.3 Pentacene-based low voltage OFETs with anodized SiO_2 and Ta_2O_5 gate dielectrics

2.3.1 EXPERIMENTS

Pentacene-based top-contact OFETs were fabricated using three different gate dielectrics: a 470 Å SiO_2, a 1,700Å Ta_2O_5, and an 800 Å Ta_2O_5. The 470 Å SiO_2, the 1,700 Å Ta_2O_5, and the 800Å gate dielectrics were obtained by anodizing an *n*-Si wafer, a sputtered Ta layer, and an e-beam evaporated Ta layer, respectively. A Pt electrode was used as the cathode. The procedures for obtaining the three gate dielectrics began when a citric acid ($C_6H_8O_7$) solution of 0.01 M was prepared using distilled water as solvent followed by immersion of the anode and the cathode. During the anodization, DC voltages were applied between the anode and the cathode by a variable power supply. The voltage was increased by 1 V every 2 min. up to 35 V and kept constant for 12 hrs. for the *n*-Si wafer, for 4.5 hrs. for the sputtered Ta layer, and for 3 hrs. for the e-beam evaporated Ta layer. The overall anodization for the *n*-Si wafer and the Ta layers are given by reaction equation (2.2) and (2.3), respectively.

$$Si + 2h^+ + 2H_2O \rightarrow SiO_2 + 2H^+ + H_2 \quad (2.2)$$

$$2Ta + 2h^+ + 5H_2O \rightarrow Ta_2O_5 + 2H^+ + 4H_2 \quad (2.3)$$

The thickness of each of the gate dielectrics was measured by a variable angle and wavelength ellipsometer, and the actual capacitance was measured by a high frequency *CV* at 1 MHz using a metal-oxide-Si (MOS) capacitor [15].

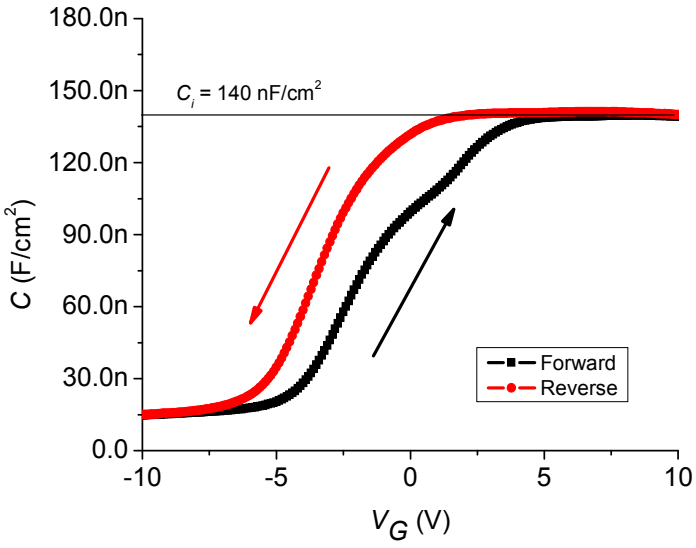
In order to functionalize the surface of the three anodized gate dielectrics, three surface treatment agents were used. An octyltrichlorosilane [OTS, $CH_3(CH_2)_7SiCl_3$] treatment was employed to the 470 Å SiO_2 substrate [75,76]. The 1,700Å Ta_2O_5 and the 800 Å Ta_2O_5 substrates were treated with hexamethyldisilazane [HMDS, $(CH_3)_3SiNH(CH_3)_3$] [77] and mono-dodecyl phosphate [MDP, $(C_{12}H_{25}O)P(O)(OH)_2$] [78,79].

As-purchased pentacene was thermally sublimed onto the prepared substrates under a vacuum of 1.2×10^{-7} torr. The deposition rate was kept at 0.1 Å/s up to 60 Å and increased to 0.5 ~ 0.7 Å/s for an additional 290 Å without substrate heating. The device fabrication was completed with an evaporation of 500 Å thick patterned Au layer for the source electrode and the drain electrode. The devices had the channel length (L) of 50 μm and the channel width (W) of 500 μm.

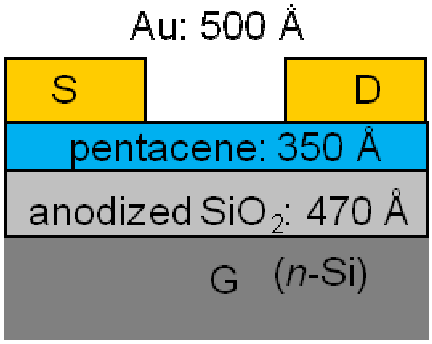
2.3.2 RESULTS

2.3.2.1 OFETs with the anodized SiO_2 gate dielectric

The anodization of the *n*-Si wafer resulted in a 470 Å SiO_2 layer with the root mean square (RMS) surface roughness of 4.6 Å, which is comparable to that of thermally grown SiO_2 (2.6 Å). Using a high frequency *CV* measurement at 1 MHz, the capacitance of the anodized SiO_2 gate dielectric was calculated to be 140 nF/cm^2 [Fig. 2.2 (a)]. The final structure of the device is shown in Fig. 2.2 (b).

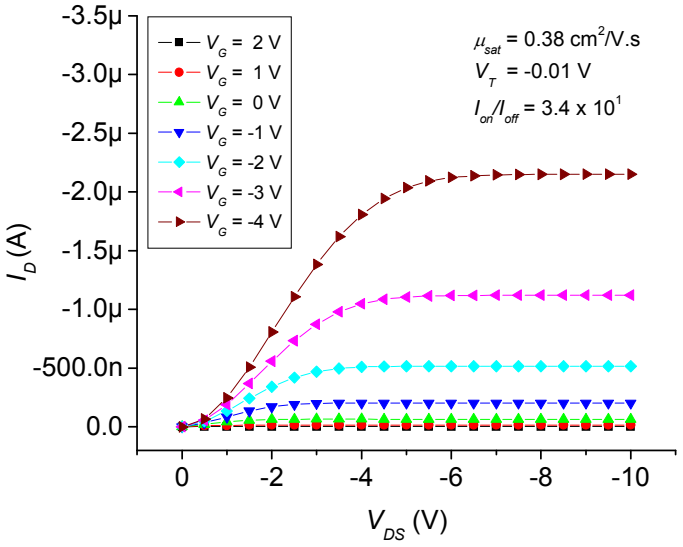


(a) High frequency *CV* measurement at 1 MHz for the anodized SiO_2 layer

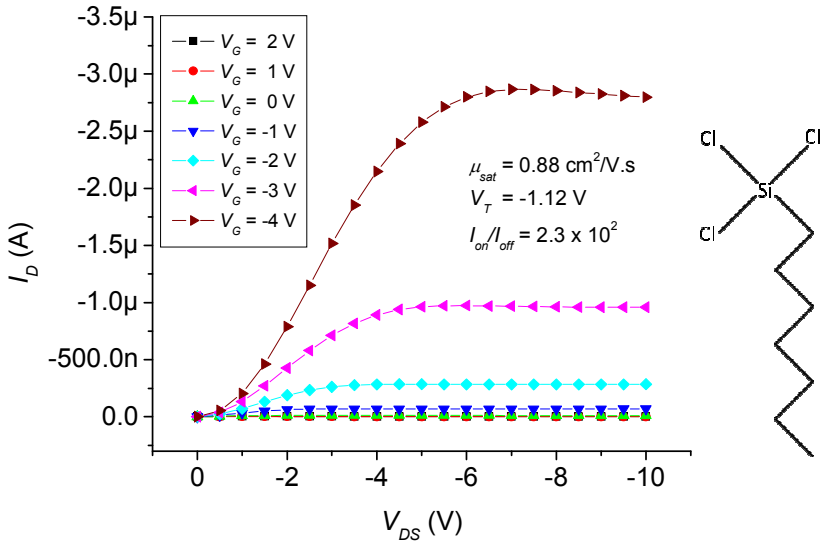


(b) Device structure of the OFET with the anodized SiO_2; $L = 50\ \mu m$, $W = 500\ \mu m$

Fig. 2.2 (a) High frequency *CV* measurement at 1 MHz for the anodized SiO_2, whose capacitance is calculated to be 140 nF/cm^2 (b) The device structure of the OFET with the anodized SiO_2 as the gate dielectric.



(a) Output characteristics of the untreated device



(b) Output characteristics of the OTS-treated device

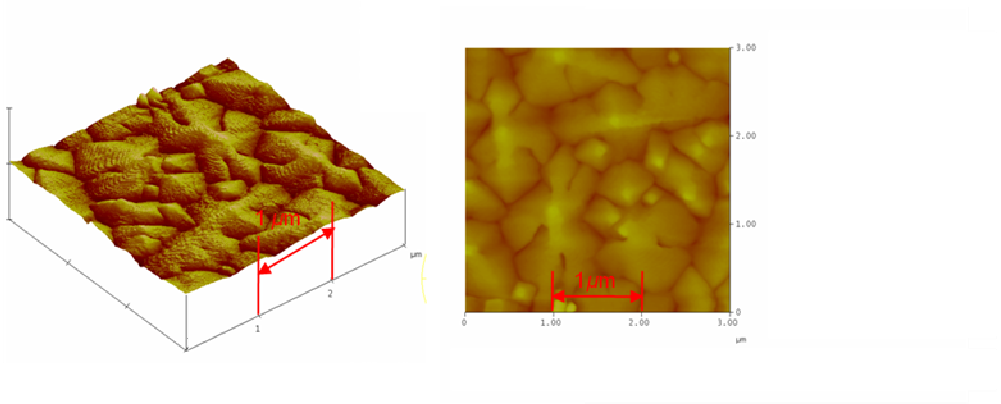
Fig. 2.3 Comparison of the output characteristics: (a) the untreated and (b) the OTS-treated OFET with the anodized SiO_2 gate dielectric. The inset represents the molecular structure of OTS.

The output characteristics of the untreated and the OTS-treated OFET are shown in Fig. 2.3. Even though both of the devices are operated at very low drain voltage $V_{DS} \leq$ -10 V and gate voltage $V_G \leq 4$ V, the saturation mobility is calculated to be 0.38 cm^2/V.s and 0.88 cm^2/V.s for the untreated and the OTS-treated device, respectively. It is obvious that the OTS treatment improves the saturation mobility by a factor of 2.3. This increase in the saturation mobility is due to a larger grain size of the pentacene thin film, which results from the reduced surface energy by the OTS SAM that favors enhanced ordering of pentacene molecules. AFM images demonstrate the grain size difference between the untreated device and the OTS-treated device (Fig. 2.4). The threshold voltage V_T increases with the OTS treatment by -1.01 V: from -0.01 V to -1.12 V. This threshold voltage increase likely results from the substantial capacitance of the OTS SAM, which results from the relatively long molecular length of an OTS molecule.

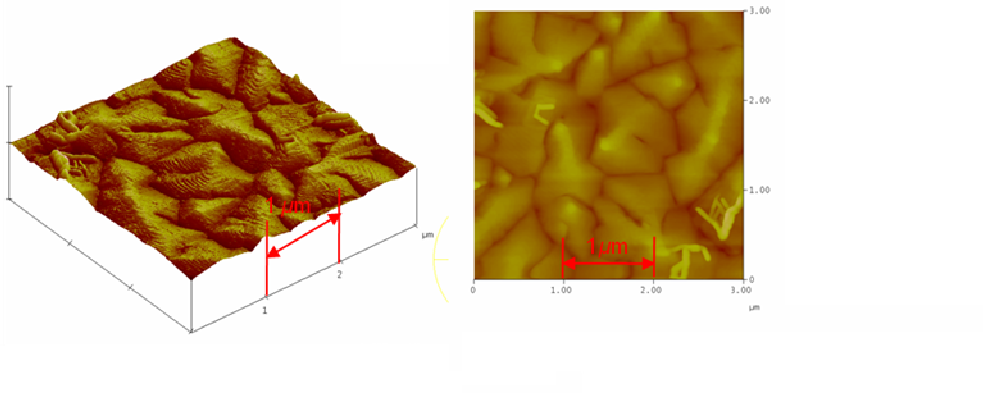
The OTS treatment also reduces gate leakage current by approximately an order of magnitude (Fig. 2.5). For example, the gate leakage current drops off by 93%: from -11 nA to – 800 pA at $V_{DS} = 0$ V and $V_G = -4$ V. The decrease in gate leakage current is indicative of the OTS SAM as an effective barrier that keeps charge carriers from tunneling through the relatively leaky anodized SiO_2 gate dielectric.

The improved ratio of I_{on}/I_{off} ratio is also understandable in terms of the OTS SAM as a coating layer. Without the OTS SAM, the total off current is the sum of pentacene-bulk component and the interface component between the pentacene thin film and the SiO_2 layer (-63.2 nA). However, with the OTS SAM, the off current comprises only the pentacene-bulk component (-12.2 nA). Because the OTS-treated device has a

higher on current (-2.78 μA) than the untreated device (-2.15 μA), the OTS-treated device shows a higher I_{on}/I_{off} ratio than the untreated device by nearly an order of magnitude. The results of the OTS treatment are recapitulated in Table 2.1.

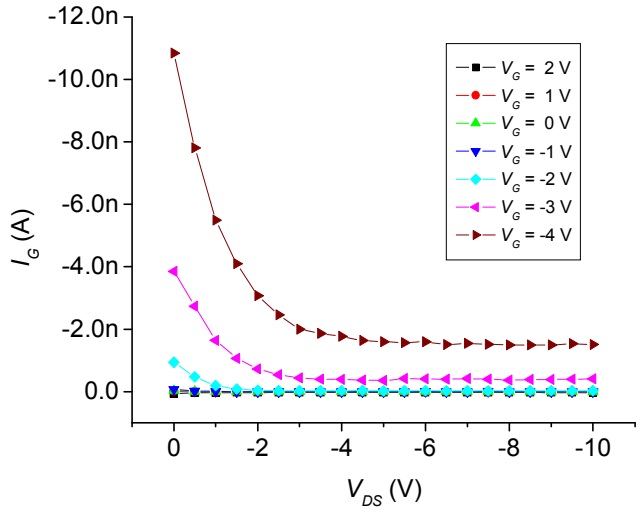


(a) AFM images of the untreated device

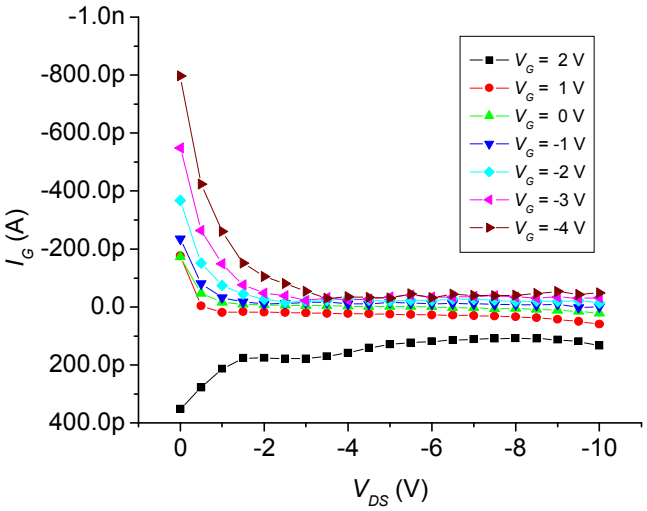


(b) AFM images of the OTS-treated device

Fig. 2.4 Comparison of pentacene morphology using AFM images: (a) the untreated device and (b) the OTS-treated device with the anodized SiO_2 gate dielectric. The AFM images demonstrate the grain size difference between the untreated device and the OTS-treated device.



(a) Gate leakage curents of the OTS-treated device



(b) Gate leakage currents of the OTS-treated device

Fig. 2.5 Comparison of gate leakage currents: (a) the untreated device and (b) the OTS-treated device with the anodized SiO_2 gate dielectric. The OTS treatment reduces the gate leakage currents significantly.

	No Treatment	OTS Treatment	Effects of OTS Treatment
$\mu_{sat.}$ (cm^2/Vs)	0.38	0.88	↑ × 2.3
V_T(V)	-0.01	-1.12	↑ -1.11 V
I_{on}/I_{off} ratio (V_{DS} = -5 V, V_G = 0 ~ -2.5 V)	3.4×10^1	2.3×10^2	↑ $\times 10^1$
Gate leakage current: I_G(A) (V_G = -4 V, V_{DS} = 0 V)	-11 nA	- 800 pA	↓ 93 %

Table 2.1 Effects of the OTS treatment on the anodized SiO_2 gate dielectric. The OTS treatment is effective in increasing the mobility, improving the I_{on}/I_{off} ratio, and reducing the gate leakage current of the device. The increased threshold voltage is due to the substantial capacitance of the OTS SAM.

2.3.2.2 OFETs with the anodized Ta_2O_5 gate dielectric obtained from a sputtered thin Ta film

Pentacene-based top-contact OFETs were fabricated using anodized Ta_2O_5 of thickness 1,700 Å as a gate dielectric and a moderately doped *n*-Si wafer with resistivity ranging from 0.1 to 1.0 Ω.cm as the gate electrode. The Ta_2O_5 gate dielectric was obtained by anodizing a thin Ta film sputtered onto the *n*-Si substrate. Before the anodization, the thin Ta film was annealed for 1 min. at 900 °C in order to get a more dense ordering of Ta atoms. The resulting device structure is shown in Fig. 2.6 along with the surface morphology of the pentacene and anodized Ta_2O_5 layers by atomic force microscopy (AFM). The RMS roughness of the anodized Ta_2O_5 surface was confirmed to be 22.9 Å atomic, which is much worse than that of conventional thermally grown SiO_2 2.6 Å. The relatively small pentacene grain size is most probably due to its dependence on the Ta_2O_5 morphology.

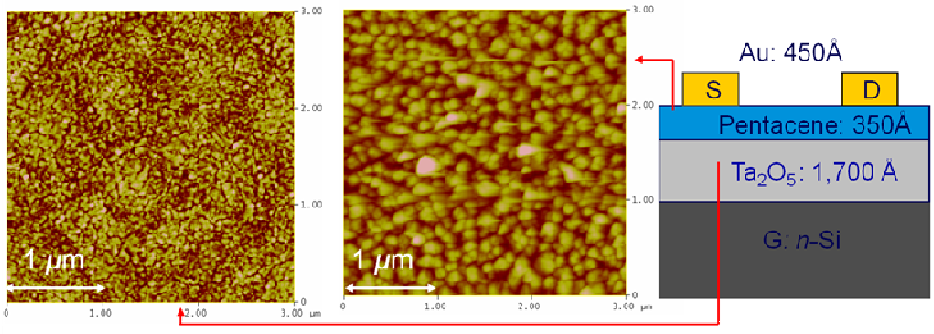


Fig. 2.6 Device structure (L = 50 μm, W = 500 μm) of the OFET with the anodized Ta_2O_5 layer as the gate dielectric (right). The AFM images show the surface morphology of the Ta_2O_5 (left) and the pentacene layer (center).

The thickness of the anodized Ta_2O_5 gate dielectric was measured by a variable angle and wavelength ellipsometer as well as a scanning electron microscope (SEM). Table 2.2 presents three possible thickness values measured by the variable angle and wavelength ellipsometer. The thickness of the Ta_2O_5 layer was found to be about 1,670 Å for all the three cases, which agreed quite well with the value verified by SEM (1,700 Å) illustrated in Fig. 2.7. From the thickness data, it is highly likely that during the anodization, the sputtered Ta layer had oxidized completely and that the anodization process was halted before the *n*-Si layer started to oxidize because of the slow anodization rate of the *n*-Si substrate: 470 Å/12 hrs.

	n-Si	Ta	Ta_2O_5
Case 1	Substrate	0 ± 0.6 Å	1,679 ± 2 Å
Case 2	Substrate	0 ± 8.5 Å	1,675 ± 7 Å
Case 3	Substrate	-	1,665 ± 1 Å

Table 2.2 Possible thickness values of the anodized Ta_2O_5 layer measured by a variable angle and wavelength ellipsometer. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, MRS Symposium Proceedings 1003E (2007); accepted. Copyright 2007, Materials Research Society

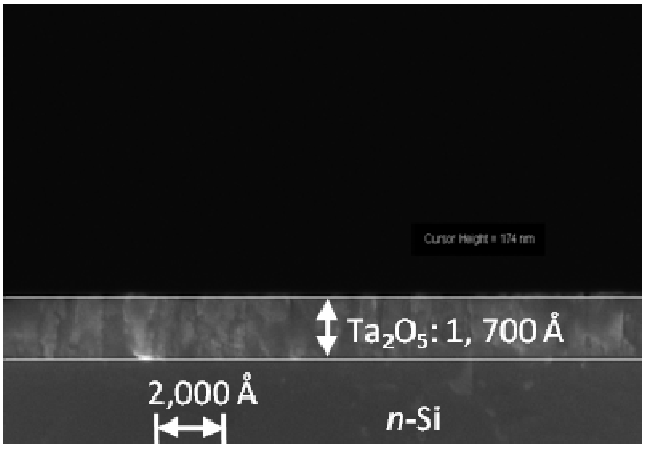
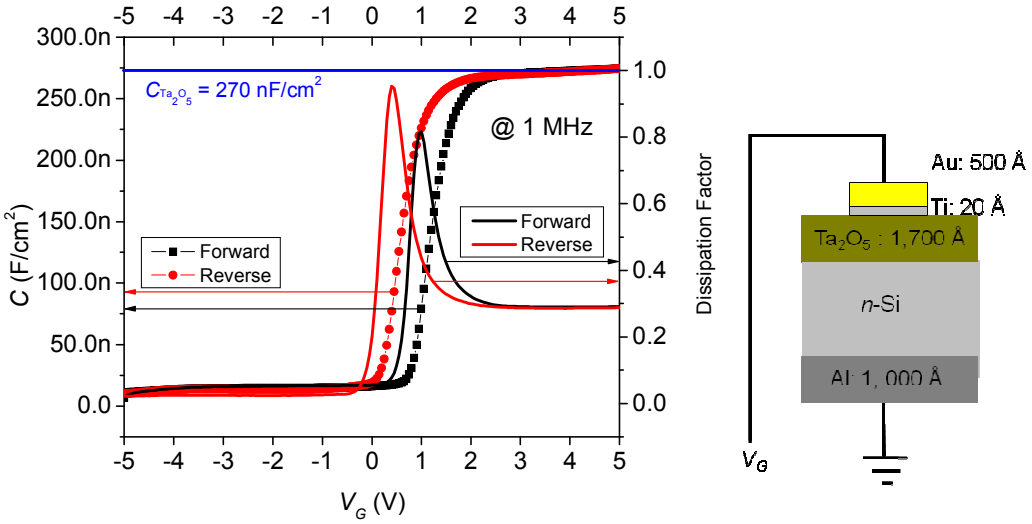


Fig. 2.7 Cross-section SEM image of the anodized Ta_2O_5 of 1,700 Å (upper) and the *n*-Si substrate (lower). The thickness value is very close to those measured by a variable angle and wavelength ellipsometer. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, MRS Symposium Proceedings 1003E (2007); accepted. Copyright 2007, Materials Research Society

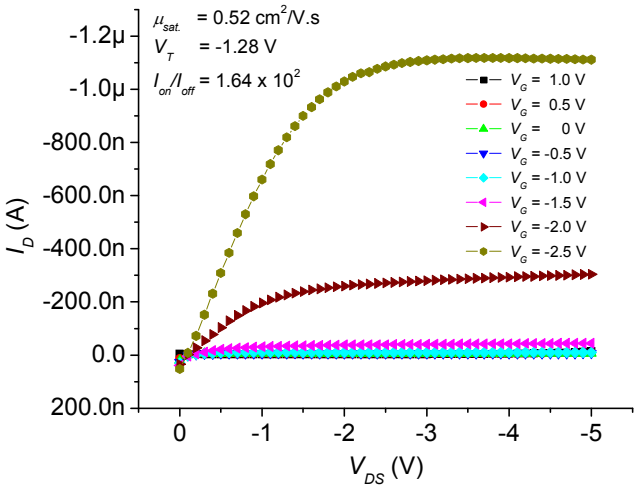
The capacitance of the Ta_2O_5 layer was measured using a metal/oxide/*n*-Si (MOS) capacitor that consisted of the top Au/Ti electrode (500 Å/20 Å), Ta_2O_5 (1,700 Å), *n*-Si, and bottom Al electrode (1,000 Å) [Fig. 2.8 (b)]. A high frequency CV measurement at 1 MHz exhibited an accumulation capacitance of 270 nF/cm^2 that is identical to the capacitance of the Ta_2O_5 layer [Fig. 2.8 (a)]. In addition, the dissipation factor was kept below 1 over the whole voltage sweep range, which means that the anodized Ta_2O_5 layer possesses good properties as a gate dielectric.



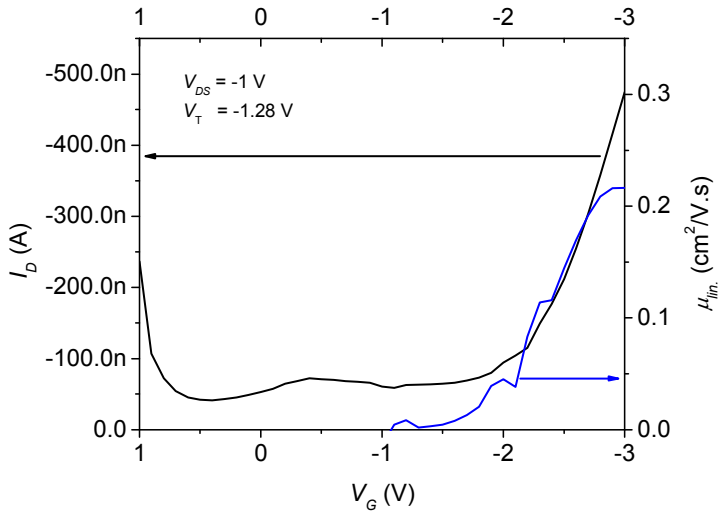
(a) (b)

Fig. 2.8 (a) High frequency *CV* measurement at 1 MHz (b) Structure of metal (Ti/Au)/oxide (Ta_2O_5)/n-Si capacitor. The accumulation capacitance of the anodized Ta_2O_5 layer is calculated to be 270 nF/cm^2. The dissipation factor is kept below 1 over the whole voltage sweep range, which means that the anodized Ta_2O_5 layer possesses good properties as a gate dielectric. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, MRS Symposium Proceedings 1003E (2007); accepted. Copyright 2007, Materials Research Society

Fig. 2.9 presents the (a) output characteristics and (b) transfer characteristics of the device shown in Fig. 2.6. The saturation mobility $\mu_{sat.}$, threshold voltage V_T, and I_{on}/I_{off} ratio calculated from the output characteristics are 0.52 cm^2/Vs, -1.28 V, and 1.64 × 10^2, respectively. The gate-voltage-dependent liner region mobility $\mu_{lin.}$ obtained from the transfer characteristics is 0.22 cm^2/Vs at V_{DS} = -5 V and V_G = -3 V. Considering that as-purchased pentacene was used as the channel material without any purification or substrate heating, these two mobility values are quite high.



(a) Output characteristics



(b) Transfer characteristics at V_{DS} = -1 V

Fig. 2.9 (a) Output characteristics and (b) transfer characteristics at V_{DS} = -1 V of the device shown in Fig. 2.6. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, MRS Symposium Proceedings 1003E (2007); accepted. Copyright 2007, Materials Research Society

Despite the high saturation and linear region mobility, the anodized Ta_2O_5 device exhibits a relatively high gate leakage current level: -110 nA at V_{DS} = 0 V and V_G = -2.5 V, which accounts for one-tenth the drain current -1.0 μA at V_{DS} = -5 V and V_G = -2.5 V. In order to address the problem of the relatively high gate leakage current, a hexamethyldisilazane (HMDS, $C_6H_{19}NSi_2$) treatment and a mono-dodecyl phosphate (MDP, $C_{12}H_{27}O_4P$) treatment were performed on the anodized Ta_2O_5 surface.

	No Treatment	HMDS Treatment	Effects of HMDS Treatment
$\mu_{sat.}$ (cm^2/Vs)	0.12	0.14	↑ × 1.2
V_T (V)	-1.50	-0.75	↓ -0.75 V
I_{on}/I_{off} ratio (V_{DS} = -5 V, V_G = 0 ~ -2.5 V)	5.37×10^1	8.01×10^2	↑ × 10^1
Gate leakage current: I_G (A) (V_G = -3 V, V_{DS} = 0 V)	-3.8 nA	-2.3 nA	↓ 40 %

Table 2.3 Effects of HMDS treatment on the saturation mobility, threshold voltage, I_{on}/I_{off} ratio, and gate leakage current of the device shown in Fig. 2.6. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, MRS Symposium Proceedings 1003E (2007); accepted. Copyright 2007, Materials Research Society

Table 2.3 summarizes the effects of the HMDS surface treatment on the device characteristics. The gate leakage current is reduced by about 40% from the HMDS treatment: from -3.8 nA to -2.3 nA at V_G = -3 V and V_{DS} = 0 V. The HMDS treatment also results in slightly enhanced saturation mobility, decreased threshold voltage by a factor of two, and increased I_{on}/I_{off} ratio by more than an order of magnitude. The saturation mobility value that is lower than the highest value of 0.52 $cm^2/V.s$ by a factor of four is probably due to the use of a different pentacene source. The reduced threshold voltage can be explained as follows: Because of the relatively short chain length of HMDS molecule, the HMDS SAM component of the total capacitance is insignificant; therefore, the threshold voltage is mainly dependent on the increased pentacene grain size. With the larger grain size and the fewer grain boundaries, the number of trapped charges in the grain boundaries decreases. The net result is the reduced threshold voltage. The improved I_{on}/I_{off} ratio is explicable in terms of the HMDS SAM as a coating layer similar to the OTS SAM on the anodized SiO_2 gate dielectric. The relatively rough surface of the Ta_2O_5 layer seems to be responsible for the smaller grain size of the pentacene layer, which makes it difficult to distinguish the grain size difference between the HMDS-treated and the untreated devices. Even though no significant grain size difference is found between these two devices, the self-assembled monolayer (SAM) of HMDS molecules is deemed to be effective in ordering pentacene molecules and reducing leakage current through the anodized Ta_2O_5 gate dielectric. It is not clear how HMDS molecules are attached to the surface of the anodized Ta_2O_5 surface. One possibility is

that HMDS molecules combine with hydroxyl groups (-OH) incorporated into the Ta_2O_5 layer during the anodization, replacing the hydrogen atom of the hydroxyl group.

The effects of the MDP surface treatment are summed up in Table 2.4. Most of all, a significant decrease in gate leakage current is observable; for instance, the gate leakage current is reduced by 74 % at V_G = -3 V and V_{DS} = -5 V: from -5.0 nA to -1.3 nA (Fig. 2.10). In addition, the values of the saturation mobility are relatively low, but they seem to suggest an increase by a factor of 1.6: from 1.00×10^{-3} $cm^2/V.s$ to 1.6×10^{-3} $cm^2/V.s$. The MDP treatment also increases the I_{on}/I_{off} ratio by an order of magnitude, which is consistent with the increased threshold voltage by -0.83 V: from 0.83 V to 0 V. The increased threshold voltage seems to result from the substantial capacitance of the MDP SAM due to its relatively long chain length. The structures of an HMDS molecule and an MDP molecule are presented in Fig. 2. 11; the molecular length difference is conceivable between the two molecules. As for the bonding mechanism of MDP molecules to the anodized Ta_2O_5 surface, the phosphate head groups ($-PO_4$) are considered to form a coordinate covalent bond with the Ta atoms of Ta_2O_5. Two adjacent adsorbed MDP molecules are believed to bind weakly with each other through a hydrogen bond, forming a SAM on the anodized Ta_2O_5 surface [17].

	No Treatment	MDP Treatment	Effects of MDP Treatment
$\mu_{sat.}$ (cm^2/Vs)	1.00×10^{-3}	1.6×10^{-3}	↑ × 1.6
V_T(V)	0.83	0	↑ -0.83 V
I_{on}/I_{off} ratio (V_{DS} = -5 V, V_G = 0 ~ -2.5 V)	5.3×10^{0}	5.3×10^{1}	↑ × 10^{1}
Gate leakage current: I_G (V_G = -3 V, V_{DS} = -5 V)	-5.0 nA	-1.3 nA	↓ 74 %

Table 2.4 Effects of MDP treatment on the saturation mobility, threshold voltage, I_{on}/I_{off} ratio, and gate leakage current of the device shown in Fig. 2.6.

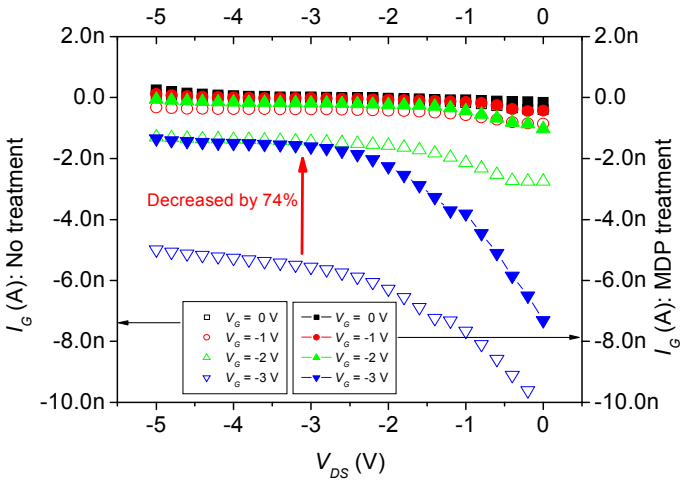
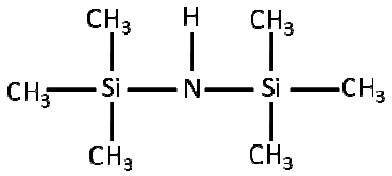
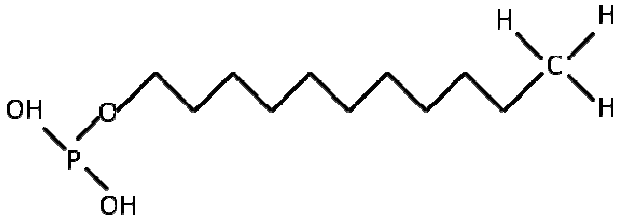


Fig. 2.10 Comparison of the gate leakage current with and without the MDP surface treatment in the device shown in Fig. 2.6: the MDP treatment reduces the gate leakage current by a significant amount.



(a) Structure of an HMDS molecule



(b) Structure of an OTS molecule

Fig. 2.11 Molecular structure of (a) HMDS and (b) OTS: the molecular length difference is conceivable between the two molecules.

2.3.2.3 OFETs with the anodized Ta_2O_5 gate dielectric obtained from an e-beam evaporated Ta thin film

Pentacene-based top-contact OFETs were fabricated using an 800 Å anodized Ta_2O_5 gate dielectric and a 90 Å Ta gate electrode. The Ta_2O_5 gate dielectric was obtained by anodizing a thin Ta layer (600 Å) e-beam evaporated onto an *n*-Si substrate with resistivity ranging from 0.1 to 1.0 Ω.cm. A 3 hr. anodic oxidation formed the anodized Ta_2O_5 (800Å), leaving the 90 Å Ta layer intact. Fig. 2.12 presents the resultant device structure and the surface morphology of the anodized Ta_2O_5 gate dielectric. The AFM image reveals that the RMS roughness of the Ta_2O_5 layer is 1.3 Å, which is comparable to that of thermally-grown dry SiO_2 (2.6 Å). The measured capacitance of the anodized Ta_2O_5 layer using an MOS capacitor was 325 nF/cm^2, from which the dielectric constant $\varepsilon_{r,Ta2O5}$ was calculated to be 29 (Fig. 2.13). The MOS capacitor was composed of the top Au/Ti electrode, Ta_2O_5 (800 Å), Ta (90 Å), *n*-Si, and bottom Al electrode. During the formation of the pentacene layer, a batch of two pentacene sources were used: the first source was sublimed onto a set of untreated and HMDS-treated samples, the second source onto a set of untreated and MDP-treated samples.

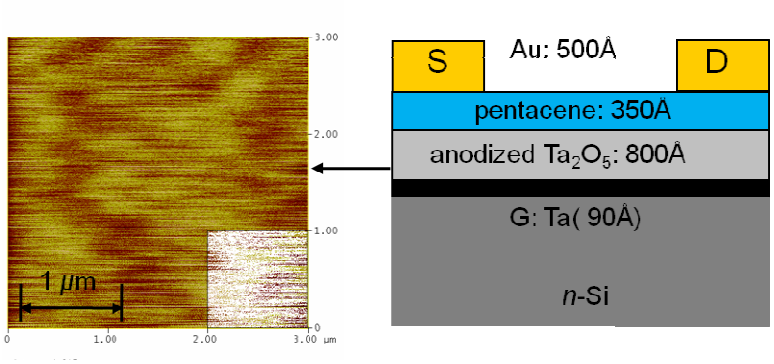


Fig. 2.12 Device structure (L = 50 μm, W = 500 μm) of the OFET with the anodized Ta_2O_5 layer as the gate dielectric. The RMS surface roughness of the Ta_2O_5 layer is 1.3 Å, which is comparable to that of thermally-grown SiO_2 (2.6 Å).

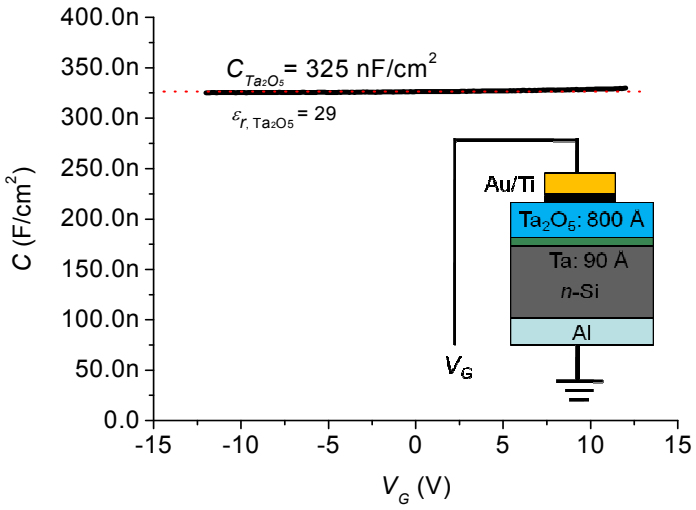
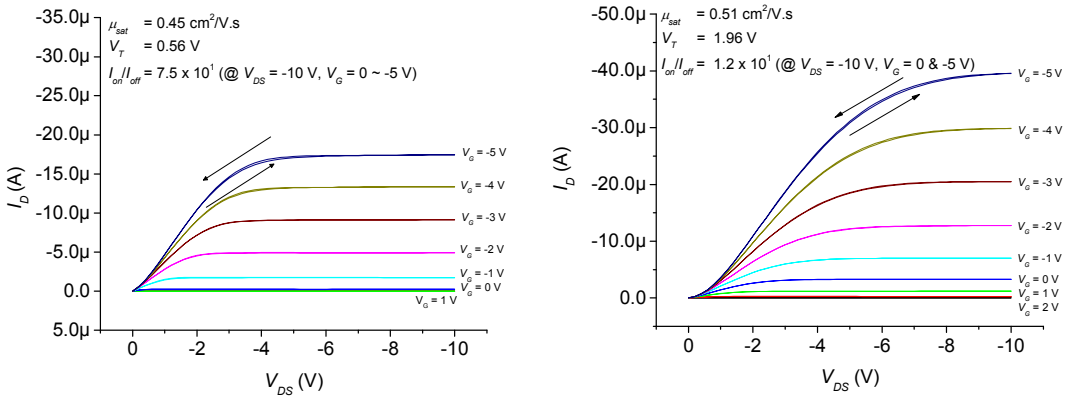
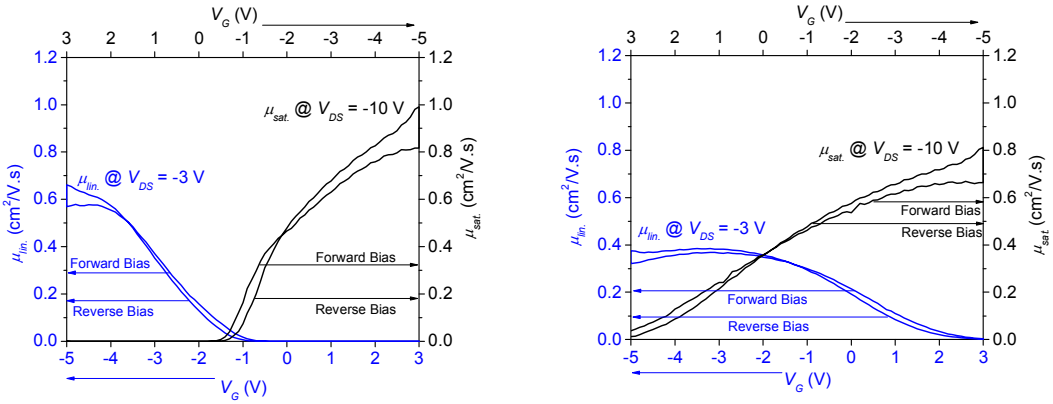


Fig. 2.13 High frequency CV measurement at 1 MHz using a MOS capacitor [Au/Ti – Ta_2O_5 (800 Å) – Ta (90 Å) – n-Si – Al], from which the capacitance of the anodized Ta_2O_5 layer is found to be 325 nF/cm^2.



(a) Untreated device (b) HMDS-treated device

Fig. 2.14 Output characteristics of (a) the untreated and (b) HMDS-treated devices. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, Appl. Phys. Lett. 91, 193509 (2007). Copyright 2007, American Institute of Physics



(a) Untreated device (b) HMDS-treated device

Fig. 2.15 Linear and saturation mobility calculated from transfer characteristics of (a) the untreated and (b) HMDS-treated devices, where only the capacitance of the Ta_2O_5 (CTa_2O_5) is considered. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, Appl. Phys. Lett. 91, 193509 (2007). Copyright 2007, American Institute of Physics

Fig. 2.14 shows the output characteristics of (a) the untreated and (b) HMDS-treated devices, in which no significant hystereses are observable. The linear region (at V_{DS} = -3 V) and saturation (at V_{DS} = -10 V) mobility values calculated from the transfer characteristics are presented in Fig. 2.15.

In the case of the untreated device, the saturation mobility at V_G = - 5 V calculated from the output characteristics and the transfer characteristics are 0.45 cm^2/V.s and 0.82 cm^2/V.s, respectively. The linear region mobility at V_{DS} = -3 V and V_G = - 5 V is calculated to be 0.34 cm^2/V.s. Considering that as-purchased pentacene was used as the channel material with no purification or substrate heating, these mobility values are quite high. The I_{on}/I_{off} ratio of the device is 7.5×10^1: I_D (V_{DS} = - 10 V, V_G = -5 V) = -17.4 μA and I_D (V_{DS} = -10 V, V_G = 0 V) = -0.23 μA. Since the gate leakage current measured at V_{DS} = -10 V and V_G = 0 V is 1 n A, the relatively high off current has its origin in the pentacene layer or the pentacene-dielectric interface rather than in the leakage through the anodized Ta_2O_5 gate dielectric, which explains the positive threshold voltage of 0.56 V. The HMDS-treated device exhibits the saturation mobility of 0.51 cm^2/V.s from the output characteristics and 0.66 cm^2/V.s from the transfer characteristics. The maximum linear region mobility at V_{DS} = -3 V and V_G = - 3 V is calculated to be 0.36 cm^2/V.s. As is the case with the untreated device, the HMDS-treated device shows a relatively poor I_{on}/I_{off} ratio of 1.2×10^1: I_D (V_{DS} = - 10 V, V_G = -5 V) = -39.6 μA and I_D (V_{DS} = -10 V, V_G = 0 V) = -3.3 μA. The gate leakage current at V_{DS} = -10 V and V_G = 0 V is 3 nA, which restates that the low I_{on}/I_{off} ratio is most probably due to the pentacene film. This is also consistent with the positive threshold voltage of 1.96 V.

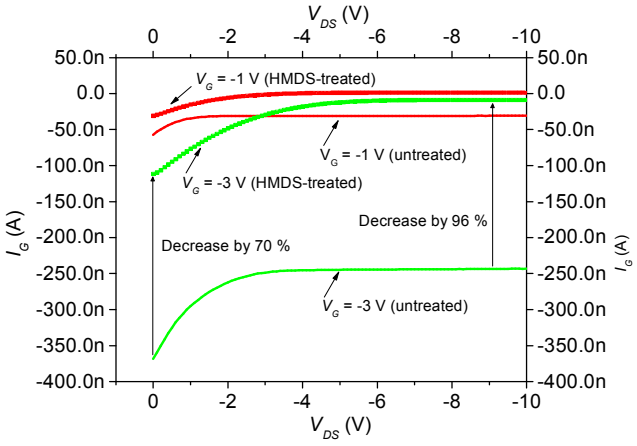
The high off currents are very likely due to the pentacene not being purified by sublimation. In other experiments with the same gate insulator and purified pentacene, I_{on}/I_{off} ratios in excess of 10^4 have been achieved. This indicates that there is no chemical interaction between Ta_2O_5 and pentacene that results in a doping effect due to the oxidation of pentacene.

In calculating the saturation and linear region mobility of the HMDS-treated device, only the capacitance of the Ta_2O_5 layer is considered. However, if the capacitance of the self-assembled monolayer of the HMDS molecules is taken into consideration, the mobility values seem to increase by a considerable amount. The measured capacitance of the anodized Ta_2O_5 layer using an MOS capacitor was found to be 325 nF/cm^2 (Fig. 2.13). Although the exact capacitance of the self-assembled monolayer of HMDS molecules was not measurable, a rough capacitance value of 1,000 nF/cm^2 could be obtained by an approximation with the dielectric constant of $\varepsilon_{r,\mathrm{HMDS}} = 2.27$ and the 2 nm chain length of an HMDS molecule [80]. Because of the substantial effect of the HMDS monolayer, the total capacitance is given by a serial combination of the anodized Ta_2O_5 layer and the HMDS monolayer, being reduced to 245 nF/cm^2. Table 2.5 summarizes the effects of the HMDS treatment on the device characteristics. All the mobility values slightly increase when the capacitance of the HMDS monolayer is ignored except for the saturation mobility calculated from the transfer characteristics; however, these values seem to improve further with the consideration of the total capacitance. The HMDS treatment also reduces the gate leakage current by more than 70 % at $V_{DS} = 0$ V and $V_G = -3$V: from -375 nA to -110 nA as shown in Fig. 2.16 (a). In addition, the HMDS

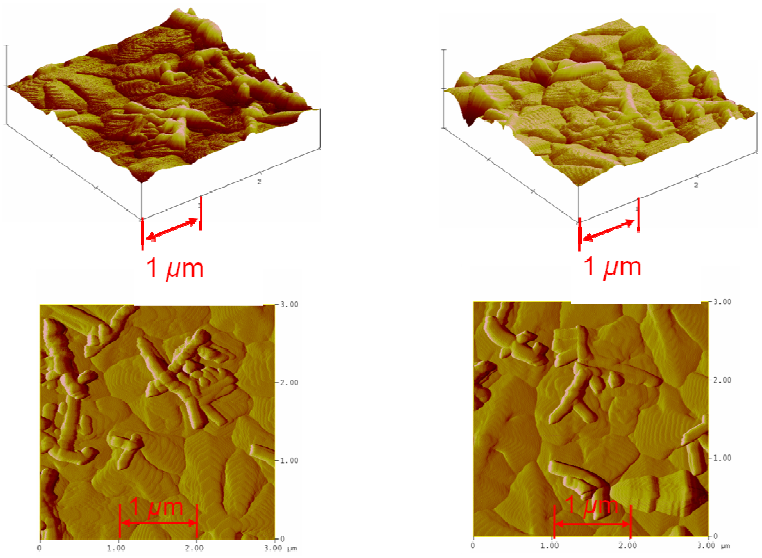
treatment is accompanied by relatively larger pentacene grain size [Fig. 2.16 (b)], which is consistent with the increased mobility values. The adsorption of HMDS molecules to the anodized Ta_2O_5 surface can be assumed in the same way as the anodized Ta_2O_5 surface obtained from the sputtered thin Ta film: HMDS molecules bond with hydroxyl groups (-OH) incorporated into the Ta_2O_5 during the anodization, replacing the hydrogen atom of the hydroxyl group.

	No Treatment	HMDS Treatment	
		$C = C_{Ta_2O_5}$	$1/C = 1/ C_{Ta_2O_5} + C_{HMDS}$
$\mu_{sat.}$ (cm^2/Vs) from output characteristics	0.45	0.51	0.67
$\mu_{sat.}$ (cm^2/Vs) from transfer characteristics	0.82	0.66	0.87
$\mu_{lin.}$ (cm^2/Vs) at V_{DS} = -3 V, V_G = -3 V	0.34	0.36	0.48
V_T (V)	0.56	1.96	·····
I_{on}/I_{off}	7.5×10^1	1.2×10^1	·····

Table 2.5 Effects of HMDS surface treatment on the pentacene-based OFET with the anodized Ta_2O_5 gate dielectric obtained from an e-beam evaporated Ta thin film. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, Appl. Phys. Lett. 91, 193509 (2007). Copyright 2007, American Institute of Physics



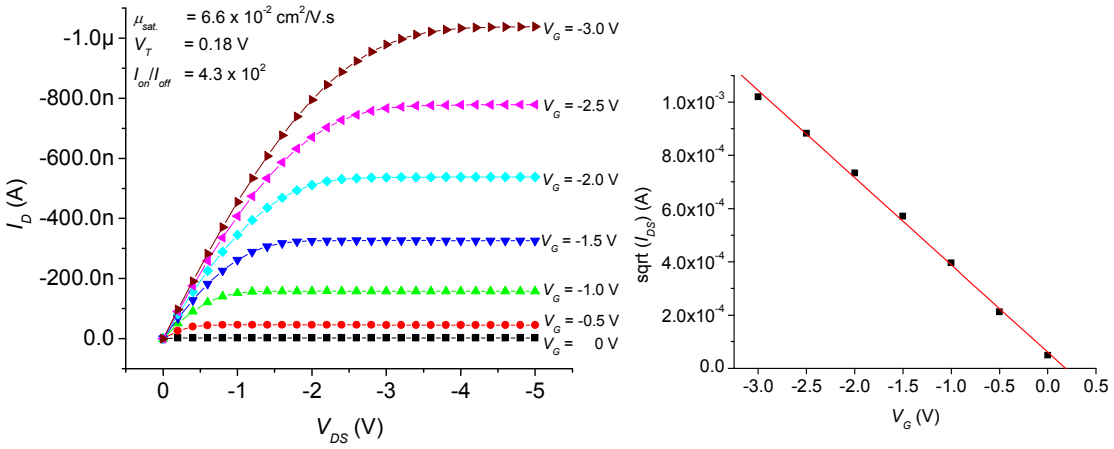
(a) Gate leakage current vs. V_{DS} at V_G = -1 V and -3 V



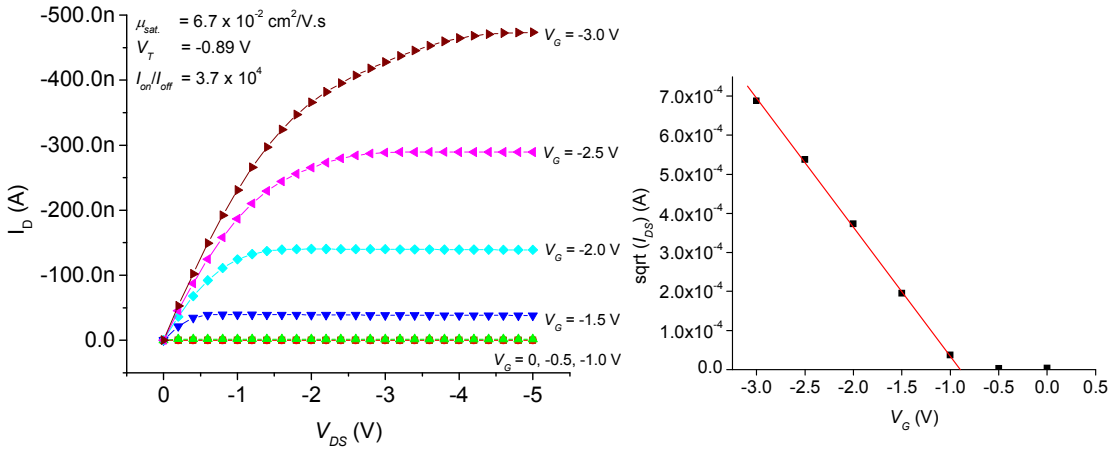
Untreated device HMDS-treated device

(b) Pentacene morphology of the untreated and HMDS-treated devices

Fig. 2.16 (a) Gate leakage current vs. V_{DS} at V_G = -1 V and -3 V (b) Pentacene morphology of the untreated and HMDS-treated devices. Reprinted with permission from Yeon Taek Jeong and Ananth Dodabalapur, Appl. Phys. Lett. 91, 193509 (2007). Copyright 2007, American Institute of Physics



(a) Untreated device



(b) MDP-treated device

Fig. 2.17 Output characteristics along with $\sqrt{I_{DS}}$ vs. V_G plot of (a) the untreated device and (b) the MDP-treated device.

Fig. 2.17 presents the effects of the mono-dodecyl phosphate (MDP) treatment on the device characteristics, where the output characteristics and the $\sqrt{I_{DS}}$ vs. V_G plot of (a) the untreated device and (b) the MDP-treated device are shown. Even though the drain currents are higher in the untreated device than in the MDP-treated device, the saturation mobility values are nearly the same: 6.6×10^{-2} cm^2/V.s for the untreated device, and 6.7×10^{-2} cm^2/V.s for the untreated device. Since these mobility values are calculated only with the consideration of the capacitance of the Ta_2O_5 layer ($C_{Ta_2O_5}$ = 325 nF/cm^2), the saturation mobility of the MDP-treated device is expected to be somewhat higher than the 6.7×10^{-2} cm^2/V.s if the capacitance of the MDP SAM is taken into consideration. The capacitance of the MDP SAM (C_{MDP}) can be approximately calculated by using the following relation: for a material, its refractive index n is given by

$$n = \sqrt{\mu_r \varepsilon_r} \tag{2.4}$$

where ε_r represents its relative permittivity, μ_r its relative permeability. For a nonmagnetic material ($\mu_r = 1$), this relation is reduced to

$$\varepsilon_r = n^2 \tag{2.5}$$

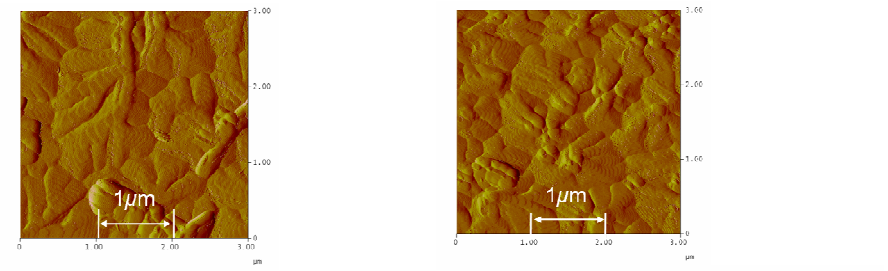
With its refractive index of the n = 1.424, the dielectric constant of the MDP SAM ($\varepsilon_{r,MDP}$) is estimated to be 2.03 [81]. If the chain length of an MDP molecule is assumed to be 2 nm, the capacitance of the MDP SAM (C_{MDP}) is approximately 900 nF/cm^2 [37]. As a result, the total capacitance (C_{total}) is found to be 239 nF/cm^2. The resulting saturation mobility of the MDP-treated device is 9.0×10^{-2} cm^2/V.s, which is significantly higher than the mobility of the untreated device 6.7×10^{-2} cm^2/V.s by a factor of 1.34.

	No Treatment	MDP Treatment	
		$C_{total} = C_{Ta_2O_5}$	$1/C_{total} = 1/C_{Ta_2O_5} + 1/C_{MDP}$
$\mu_{sat.}$ (cm^2/Vs) from output characteristics	6.6×10^{-2}	6.7×10^{-2}	9.0×10^{-2}
V_T (V)	0.18	-0.89	·····
I_{on}/I_{off}	4.3×10^2	3.7×10^4	·····

Table 2.6 Effects of MDP surface treatment on the pentacene-based OFET with the anodized Ta_2O_5 gate dielectric obtained from the e-beam evaporated Ta thin film. With the consideration of the capacitance of the MDP SAM, the mobility is further increased by a factor of 1.34. The OTS treatment is also effective in improving the I_{on}/I_{off} ratio due to the nature of the OTS SAM as a coating layer. The increased threshold voltage results from the significant capacitance of the OTS SAM.

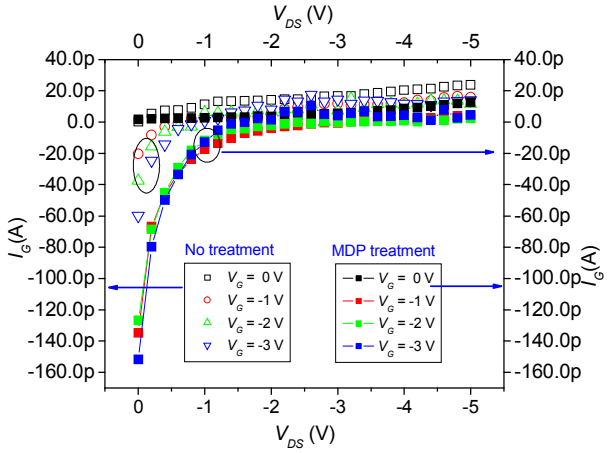
Table 2.6 summarizes the device performance with and without the MDP-treatment. The table also shows that the MDP-treatment increases the threshold voltage V_T by -1.07 V as well as improves the I_{on}/I_{off} ratio nearly by two orders of magnitude. Considering that there is no noticeable grain size difference between the two devices, the increased threshold voltage in the MDP-treated device is attributable to the capacitance of the MDP SAM [Fig. 2.18(a)]. The improved I_{on}/I_{off} ratio is explainable by the off-current difference between the two devices: at V_{DS} = -5 V and V_G = 0 V, the drain currents of the untreated and MDP-treated devices are -2.4 nA and -13 pA, respectively. In addition, Fig. 2.18 (b) proves that the gate leakage current of the untreated device is 24 pA at V_{DS} = -5 V and V_G = 0 V, which is much smaller than the off current of the -2.4 nA. In other words, in the case of the MDP-treated device, the off current is dominated by the bulk

component (-13 pA) since the MDP SAM acts as a coating layer that nullifies the interface component.



Untreated device MDP-treated device

(a) Pentacene morphology



(b) Gate leakage current

Fig. 2.18 (a) Surface morphology of the pentacene layer in the untreated device and the MDP-treated device (b) Gate leakage current vs. VDS at VG = 0, -1, -2, and -3 V.

2.4 Conclusions

Despite the significant advances in fabricating OFETs with feasibly high carrier mobility, their generally high operating voltages have yet to be lowered to practical levels. This chapter has covered the use of three different anodized gate dielectrics to realize the pentacene-based low voltage *p*-channel OFETs. The three anodized gate dielectrics were a 470 Å SiO_2, a 1,700 Å Ta_2O_5, and an 800 Å Ta_2O_5 obtained from an *n*-Si wafer, a sputtered Ta layer, and an e-beam evaporated Ta layer, respectively. In order to improve the device performance, three types of SAM treatments were carried out: an octyltrichlorosilane (OTS) treatment on the anodized SiO_2 gate dielectric, an HMDS (hexamethyldisilazane) treatment, and an MDP (mono-dodecyl phosphate) treatment on both of the anodized Ta_2O_5 gate dielectrics.

The anodization of the *n*-Si wafer formed a 470 Å SiO_2 layer with an RMS surface roughness of 4.6 Å and a capacitance of 140 nF/cm^2. Using the 470 Å anodized SiO_2 layer as the gate dielectric, devices with the saturation mobility of 0.38 cm^2/V.s, threshold voltage of -0.01 V, and I_{on}/I_{off} ratio of 3.4×10^1 at $V_{DS} \leq$ -10 V and gate voltage $V_G \leq$ -4 V, were achieved. The OTS treatment on the SiO_2 surface resulted in the improved saturation mobility of 0.88 cm^2/V.s and I_{on}/I_{off} ratio of 2.3×10^2 along with the reduced gate leakage by 93%: from -11 nA to -800 pA at V_{DS} = 0 V and V_G = -4 V. Meanwhile, the threshold voltage increased by -1.01 V: from -0.01 V to -1.12 V. The improved saturation mobility was consistent with the larger grain size of pentacene in the OTS-treated device. The improved I_{on}/I_{off} ratio and the reduced gate leakage current were attributable to the nature of the OTS SAM as a coating layer that reduces the interface

component of the total off current as well as prevents charge carriers from tunneling through the relatively leaky anodized SiO_2 gate dielectric. The increase in threshold voltage was due to the substantial capacitance of the OTS SAM.

The 1,700 Å anodized Ta_2O_5, which was obtained from the sputtered Ta thin film, exhibited a relatively poor RMS surface roughness of 22.9 Å and a capacitance of 270 nF/cm^2. The devices with the 1,700 Å anodized Ta_2O_5 exhibited the saturation mobility of 0.52 cm^2/V.s, threshold voltage of -1.28 V, and I_{on}/I_{off} ratio of 1.64×10^2 at $V_{DS} \leq$ -5 V and gate voltage $V_G \leq$ -2.5 V. The gate-voltage-dependent linear region mobility was calculated to be 0.22 cm^2/V.s at V_{DS} = -5 V and -3 V. Considering that the as-purchased pentacene was used and the grain size of pentacene was deeply dependent on the poor surface morphology of the anodized Ta_2O_5, the saturation and linear region mobility are quite high. Despite these high mobility values, however, the gate leakage current of the devices was fairly high, e.g., -110 nA at V_{DS} = 0 V and V_G = -2.5 V, which was nearly equal to one-tenth the drain current at V_{DS} = -5 V and V_G = -2.5 V. In order to address the problem of the relatively high gate leakage current, the HMDS and MDP treatments were implemented on the anodized Ta_2O_5 surface. The HMDS treatment reduced gate leakage by 40%, slightly improved the saturation mobility by 17%, decreased the threshold voltage by -0.75 V (from -1.50 V to -0.75 V), and enhanced the I_{on}/I_{off} ratio by an order of magnitude. The improved saturation mobility resulted from the larger grain size of pentacene from the HMDS treatment. The reduced threshold voltage was explainable by the larger grain size of pentacene with the relatively short chain length of an HMDS molecule; because of the relatively short chain length of an HMDS molecule, the

effective capacitance of the HMDS SAM is negligible. Consequently, the threshold voltage decreases with the larger pentacene grains, which have fewer charge-carrier traps than the smaller grains. The improved I_{on}/I_{off} ratio and the reduced gate leakage current, as is the case with the OTS treatment on the 470 Å anodized SiO_2, were explicable in terms of the HMDS SAM as a coating layer on the Ta_2O_5 surface. As for the MDP-treated devices, the gate leakage current significantly decreased, e.g., by 74% at V_G = -3 V and V_{DS} = -5 V (from -5.0 nA to -1.3 nA). The MDP treatment was also accompanied by the enhanced saturation mobility by a factor of 1.6. Moreover, the MDP treatment enhanced the I_{on}/I_{off} ratio by an order of magnitude, which was consistent with the increased threshold voltage by -0.83 V (from 0.83 V to 0 V). The increased threshold voltage resulted from the significant capacitance of the MDP SAM arising from its relatively long chain length.

Two batches of pentacene-based OFETs were fabricated using the 800 Å Ta_2O_5 as the gate dielectric that was prepared by anodizing the e-beam evaporated Ta layer, in which the capacitance of the anodized Ta_2O_5 was found to be 325 nF/cm^2. The first batch consisted of a set of untreated and HMDS-treaded devices, and the second batch onsisted of a set of untreated and MDP-treated devices. Both of the batches of devices showed the reasonable output and transfer characteristics at $V_{DS} \leq$ -10V and $V_G \leq$ -5 V. The effects of the HMDS treatments were summarized as follows: The untreated devices exhibited the saturation mobility of 0.45 cm^2/V.s, linear region mobility of 0.34 cm^2/V.s (at V_{DS} = -3 V and V_G = -3 V), threshold voltage of 0.56 V, and I_{on}/I_{off} ratio of 7.5×10^1. For the HMDS-treated device, the saturation mobility was 0.51 cm^2/V.s, the linear region mobility (at

V_{DS} = -3 V and V_G = -3 V) 0.36 cm^2/V.s, the threshold voltage 1.96 V, and the I_{on}/I_{off} ratio 1.2×10^1. The increased mobility value of the HMDS-treated device was compatible with the larger grain size of pentacene compared to that of the untreated device. The relatively poor I_{on}/I_{off} ratio resulted from the pentacene not being purified by sublimation, which was in agreement with the two positive threshold voltages of the untreated device (0.56 V) and the HMDS-treated device (1.96 V). Indeed, in other experiments with the same gate dielectric and purified pentacene, I_{on}/I_{off} ratios over 10^4 were attained. The HMDS treatment was believed to increase the mobility values by significant amounts with the consideration of the capacitance of the HMDS SAM. Under several assumptions, the capacitance of the HMDS SAM was determined to be 1,000 nF/cm^2. Because of the substantial capacitance of the HMDS SAM, the total capacitance was given by a serial combination of the anodized Ta_2O_5 layer (325 nF/cm^2) and the HMDS SAM (1,000 nF/cm^2), which was then reduced to 245 nF/cm^2. The corresponding saturation and linear region mobility were 0.67 cm^2/V.s and 0.48 cm^2/V.s, respectively. These results imply that each mobility value can increase by more than 40% with the HMDS treatment. The HMDS treatment also reduced the gate leakage current by more than 70%. The MDP treatment also had effects on the device performance. The MDP treatment changed the saturation mobility from 6.6×10^{-2} cm^2/V.s to 6.7×10^{-2} cm^2/V.s, the threshold voltage from 0.18 V to -0.89 V, and the I_{on}/I_{off} ratio from 4.3×10^2 to 3.7×10^4. However, if the capacitance of the MDP SAM was taken into consideration, the saturation mobility increased by a considerable degree; under several assumptions, the capacitance of the MDP SAM was approximately calculated to be 900 nF/cm^2, reducing the total

capacitance to 239 nF/cm^2. The resulting saturation mobility of the MDP-treated devices was 9.0 × 10^{-2} cm^2/V.s, which was equal to 1.34 times the 6.7 × 10 cm^2/V.s calculated without considering the capacitance of the HMDS SAM. The increased threshold voltage, from 0.18 V to -0.89 V, signified that the capacitance of the MDP SAM is substantial. The improved I_{on}/I_{off} ratio restated that the MDP SAM is an effective coating layer on the anodized Ta_2O_5 surface that nullifies the interface component of the total off current.

CHAPTER 3 CHARGE TRANSPORT IN PDI-8CN$_2$ BASED *N*-CHANNEL ORGANIC FIELD-EFFECT TRANSISTORS

3.1 Introduction

It is well-known that there has been remarkable progress in enhancing properties and understanding characteristics of *p*-channel organic semiconductors compared to their *n*-channel counterparts. However, it must be kept in mind that *n*-channel materials are as essential as *p*-channel materials to the realization of organic complementary circuits [23-25]. To date, there have been significant reports on synthesizing new *n*-type organic semiconductors [26,56,59-61]. Nevertheless, the charge transport mechanisms in *n*-channel OFETs are still not adequately understood. For instance, *n*-channel devices show more sensitivity to moisture and oxygen than their *p*-channel counterparts [57,58].

There are several reports concerning the synthesis and characterization of new *n*-channel materials, with the main priority being the enhancement of electron mobility and air-stability [1,23-25,57,82]. PDI-8CN$_2$, whose full name is *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide), is a quite new *n*-type organic semiconductor. This material is relatively air-stable, has a mobility that is typically > 0.1 cm^2/V.s, and has been used successfully in making short channel length bottom contact transistors as well as ring oscillators with record frequencies for organic complementary circuits [26]. Although PDI-8CN$_2$ possesses many promising attributes in terms of applications, its charge transport mechanism is not clear as is the case with better studied

organic semiconductors such as pentacene. Considering that temperature, gate voltage, and contact resistance are three major factors in deciding electrical behavior in organic devices, the knowledge of their influence on the performances of PDI-8CN_2 based OFETs can possibly pave the way for the suitable understanding of the charge transport mechanisms in PDI-8CN_2 and related *n*-channel organic semiconductors.

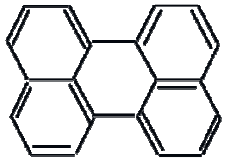
The multiple trapping and release (MTR) model is widely used in describing the charge transport in hydrogenated amorphous silicon (*a*-Si:H) [83-85], and it also looks well suited for explaining the charge transport in organic semiconductors [23,25,82,86-90]. Based on the MTR model, therefore, it is possible to derive such relations as the dependence of mobility on gate voltage and temperature, field-dependent mobility, trap density, and off current in PDI-8CN_2 based OFETs.

In organic field-effect transistors, contact resistance arises from the charge injection barrier at the interface between the source/drain electrodes and organic semiconductors. As discussed in Chapter 1, this injection barrier is usually due to poor ordering of the organic layers caused by the high surface energy of the source/drain electrodes [1,26,40,45]. Contact resistance has significant effects on the performance of OFETs, especially in the case of bottom-contact structures, as channel length is consistently scaled down. Thus, it is worth confirming how substantial the contact resistance effects are in the behavior of PDI-8CN_2 based OFETs.

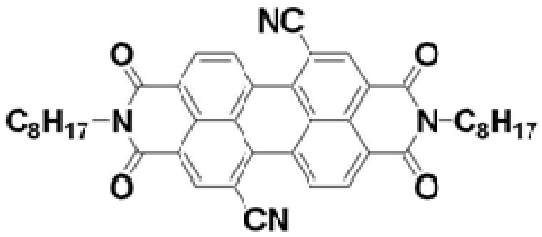
3.2 *n*-channel organic semiconductor PDI-8CN_2

A relatively new *n*-channel organic semiconductor as known as *N,N'*-bis(n-octyl)-dicyanoperylene-3,4:9,10-bis(dicarboximide), i.e., PDI-8CN_2, has a perylene core with two electron-withdrawing cyano (-CN) groups, which increase solubility by decreasing molecular planarity and stabilize charge carriers by lowering both HOMO and LUMO energy levels [23,26]. Compared to just its perylene core, the PDI-8CN_2 molecule exhibits an increased ionization potential (PI) by 1.78 eV from 5.32 eV to 7.10 eV, and an increased electron affinity (EA) by 1.01 eV from 3.29 eV to 4.3 eV. Fig. 3.1 illustrates the molecular structures of perylene and PDI-8CN_2 and the relative energy-band diagram of the two molecules.

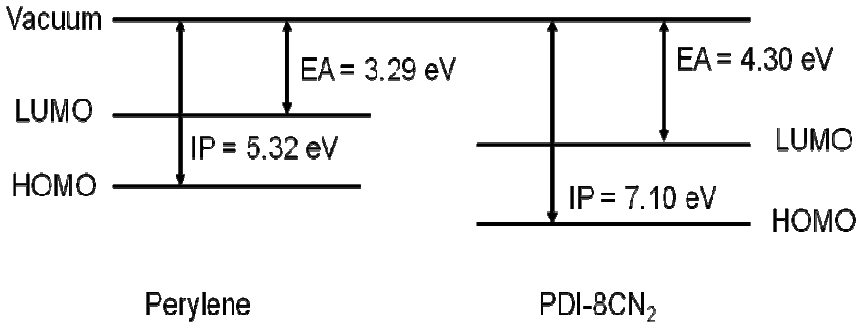
The increased electron affinity favors the injection of negative charge carriers through typical contact metals with high work functions and makes the charged material more stable with respect to oxidants such as O_2, H_2O. In fact, the ambient electrical characterization of OFETs made of PDI-8CN_2 proves to be comparable to that carried out under a vacuum.



(a) Molecular structure of perylene



(b) Molecular structure of PDI-8CN_2



(c) Energy-band diagrams for perylene and PDI-8CN_2

Fig. 3.1 Molecular structures of (a) perylene, (b) PDI-8CN_2, and (c) their relative energy-band diagram. Compared to just its perylene core, the PDI-8CN_2 molecule exhibits an increased ionization potential (PI) by 1.78 eV from 5.32 eV to 7.10 eV, and an increased electron affinity (EA) by 1.01 eV from 3.29 eV to 4.3 eV.

3.3 Dependence of the electrical behavior on temperature and gate voltage in PDI-8CN$_2$ based OFETs

3.3.1 APPLICATIONS OF THE MTR MODEL TO *N*-CHANNEL OFETS

In the MTR model, it is assumed that gate-voltage-induced surface charge σ consists of trapped charge σ_t and free carrier σ_f, and that most of the induced carriers are trapped in localized states in the forbidden gap ($\sigma_t \gg \sigma_f$) [82,87,88,90]. These assumptions give rise to the following relation:

$$\sigma = C_i V_G = \sigma_t + \sigma_f \approx \sigma_t \tag{3.1}$$

The trap states are presumed to have an exponential distribution in the forbidden gap and the determination of its density of states (DOS) is crucial in employing the MTR model. Both shallow and deep states are possible. There might also be additional trap states as depicted in Fig. 3.2.

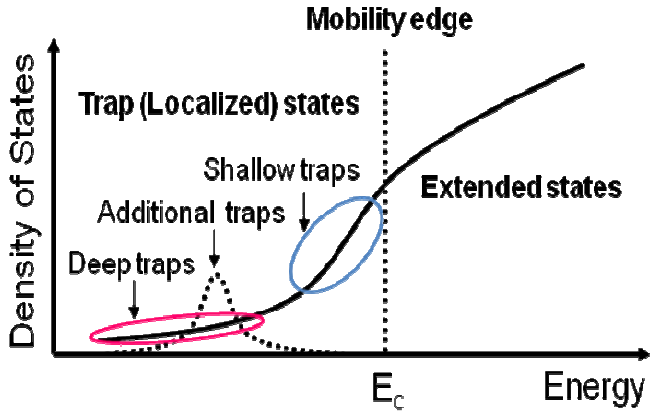


Fig. 3.2 Possible trap distributions in the forbidden energy gap; From [91]

There are three probable origins of trap states in OFETs: impurities, structural defects, and self-trappings [91]. The introduction of impurities forms new HOMO/LUMO positions independent of the matrix. Structural defects like grain boundaries generate trap sites. The formation of polaron acts like a self-trapping because it results in one or two order lower mobility compared to free carrier at room temperature.

The measured field-effect mobility μ_{FET} is related to the trap-free mobility μ_0 by

$$\mu_{FET} = \mu_0 \frac{\sigma_f}{\sigma} \tag{3.2}$$

Under a given gate voltage V_G, the Fermi-level E_f is determined by the following relation:

$$E_c - E_f = kT \ln \frac{q\mu_0 N_c}{\mu_{FET} C_i V_G} = kT \ln \frac{\mu_0 N_c}{\mu_{FET} \sigma_t} \tag{3.3}$$

where N_c denotes the surface density of states at the conduction band edge E_c. The effective density of states N_c^* is given by

$$N_c^* = 2\left(\frac{2\pi m^* kT}{h^2} \right)^{\frac{3}{2}} \tag{3.4}$$

The surface density of states N_c can be reduced to the product of $N_c^* L$, where L is the thickness of the monolayer of organic material. Assuming $m^* = 2m_o$ [92] and L = 20Å [24], the N_c value will be 1.6 × 10^{13}/cm^2 at room temperature, which is nearly temperature-independent in equation (3.3) because of the confinement in a logarithm.

The trapped charge is related to the surface density of localized states $N_t(E)$ through

$$\sigma_t = q \int_{-\infty}^{+\infty} N_t(E) f(E) dE \tag{3.5}$$

If the step function of Fermi-distribution $f(E)$ is assumed, the trap density $N_t(E_f)$ is reduced to

$$N_t(E_f) = \frac{1}{q} \frac{d\sigma_t}{dE_f} \tag{3.6}$$

In equation (3.3), the product of $\mu_0 N_c$ acts like an adjustable parameter, and the best way to determine $\mu_0 N_c$ is by minimizing the scattering of the trap distribution calculated at various temperatures.

The dependence of field effect mobility on gate voltage and temperature is roughly explained as follows: At low gate voltage, most of the injected electrons in an *n*-channel organic semiconductor layer are trapped into the localized states. With the increase in gate voltage, the Fermi-level moves toward the conduction band edge, filling more and more trap states and increasing the number of free electrons, thereby resulting in higher field effect mobility. There is a critical gate voltage that is high enough to fill all the localized trap states, at which the mobility becomes saturated. Trapped electrons are thought to be thermally released with activation energy E_a. This suggests that the field-effect mobility μ_{FET} in OFETs is dependent on both gate voltage and temperature. If the field-effect mobility is plotted as a function of the inverse of temperature, an Arrhenius relation is obtained with the activation energy E_a

$$\mu_{FET} = \mu_0 \exp\left(\frac{-E_a}{kT}\right) \tag{3.7}$$

The activation energy might have different values at high temperature and at low temperature regions, which is indicative of the distinction between deep traps and shallow traps. Usually, plotting with different gate voltages over a wide temperature range generates an isokinetic point at a certain temperature.

3.3.2 EXPERIMENTS

Devices with a bottom-contact configuration were fabricated using PDI-8CN_2 as the channel material. A bilayer gate dielectric of 2,000 Å silicon nitride (Si_3N_4) and 1,000 Å silicon dioxide (SiO_2) was formed on top of the patterned Au gate electrode, whose capacitance was calculated to be 1.69×10^{-8} F/cm^2 [62]. After defining the source/drain electrodes, a hexamethyldisilazane (HMDS) and a 1-hexadecanethiol (HDT) treatments were performed to lower the surface energy of the substrate and contact resistance, respectively, followed by the thermal evaporation of PDI-8CN_2, during which the substrate temperature was kept at 100 ºC under a vacuum of 3×10^{-7} torr. The deposition rate was maintained at 0.1 ~ 0.2 Å/s up to an initial 60 Å, and increased to 1 ~ 2 Å/s for an additional 340 Å. The channel width W and channel length L were 2,000 μm and 7.5 μm, respectively. The resulting device structure is shown in Fig. 3.3. Examined by atomic force microscopy (AFM) and scanning electron microscopy (SEM), the surface morphology of the PDI-8CN_2 thin film is presented in Fig. 3.4. The surface of evaporated PDI-8CN_2 film consists of rod-like grains, whose average length, width, and height are 450 nm, 250 nm, and 15 nm, respectively.

Variable temperature electrical measurements were performed under a vacuum < 1×10^{-4} torr using liquid nitrogen as the coolant. The temperature ranged from 80 K to 300 K with a step of 10 K. At each temperature, the transfer characteristics were obtained in the linear regime and in the saturation regime.

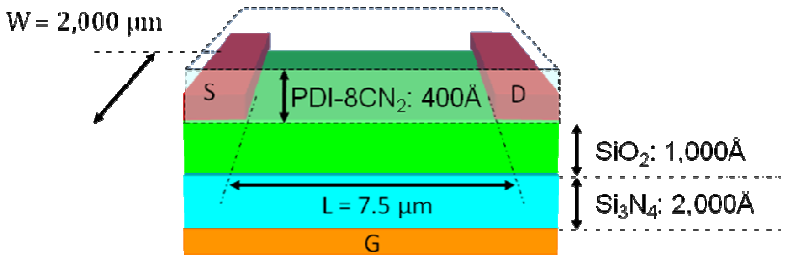
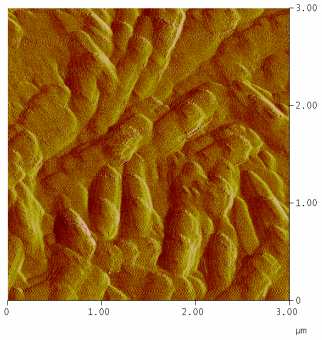
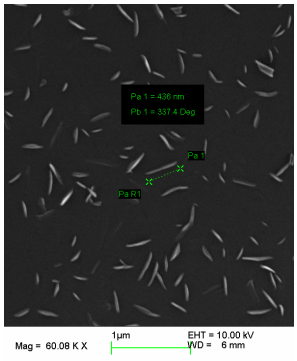


Fig. 3.3 Device structure of the PDI-$8CN_2$ based bottom-contact OFET with a bilayer gate dielectric, whose capacitance is 1.69×10^{-8} F/cm^2. The gate dielectric is made up of a 2,000 Å Si_3N_4 and a 1,000 Å SiO_2.



(a) AFM image: amplitude



(b) SEM image: × 60.08K

Fig. 3.4 Surface morphology of the evaporated PDI-$8CN_2$ thin film. The average length, width, and height of the rod-like PDI-$8CN_2$ grains are 450 nm, 250 nm, and 15 nm, respectively.

3.3.3 RESULTS

3.3.3.1 Linear regime mobility

The dependence of linear regime mobility μ_{lin} on gate voltage and temperature exhibits three distinct temperature domains: 80 K < T < 250 K; 250 K < T < 270 K; and 270 K < T < 300 K (Fig. 3.5). At 80 K to 250 K, the linear regime mobility is dependent on temperature as well as gate voltage. In this temperature regime, the activation energy E_a decreases as gate voltage increases with an isokinetic point at 250 K (Fig. 3.6), which is well explained by the MTR model. It is because, as gate voltage increases, more trap states are filled and the Fermi-level E_f approaches the band edge E_c, whose net result is reduced activation energy. However, the linear regime mobility is nearly independent of gate voltage and temperature between 250 K and 270 K, which is characterized by virtually zero activation energy. Even though it is not clear what causes the abnormality in this temperature region, one likely possibility is as follows: The hygroscopic nature of HMDS molecules introduces moisture (H_2O molecules) into the PDI-8CN_2 thin film [93]. At low temperature (80 K < T < 250 K), all the H_2O molecules are frozen, exerting no effect on the device behavior. However, the phase diagram for H_2O suggests that as temperature increases, some of the frozen H_2O molecules sublime into H_2O vapor under the vacuum of 3×10^{-7} torr, followed by forming electronegative hydroxyl $(OH)^-$ groups. The higher the temperature, the more $(OH)^-$ groups. These (OH)- groups will act as electron trapping sites. Therefore, the constant linear mobility in the temperature region (250 K < T < 270 K) is attributable to those trap sites. In other words, the effects of increased temperature and gate voltage on mobility are countered by the electron-

trapping $(OH)^-$ groups, which is observable until the temperature reaches 270 K. In the high temperature region (270 K < T < 300 K), the linear regime mobility is temperature-dependent, but very weakly gate-voltage-dependent (Fig. 3.7). This phenomenon may suggest that, at higher temperatures, temperature has a more dominant influence on linear regime mobility than gate voltage. The existence of both deep and shallow trap states is inferred from the different activation energy values in the higher and lower temperature regions (Fig.3.5).

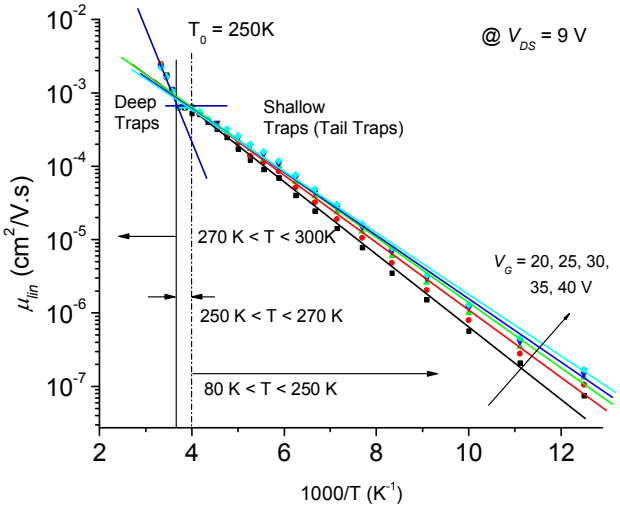


Fig. 3.5 Linear regime mobility $\mu_{lin.}$ vs. 1/T at V_{DS} = 9 V. The dependence of linear regime mobility μ_{lin} on gate voltage and temperature exhibits three distinct temperature domains: 80 K < T < 250 K; 250 K < T < 270 K; and 270 K < T < 300 K. At 80 K to 250 K, the linear regime mobility is dependent on temperature as well as gate voltage. The linear regime mobility is nearly independent of gate voltage and temperature between 250 K and 270 K, which is characterized by virtually zero activation energy. In the high temperature region (270 K < T < 300 K), the linear regime mobility is temperature-dependent, but very weakly gate-voltage-dependent.

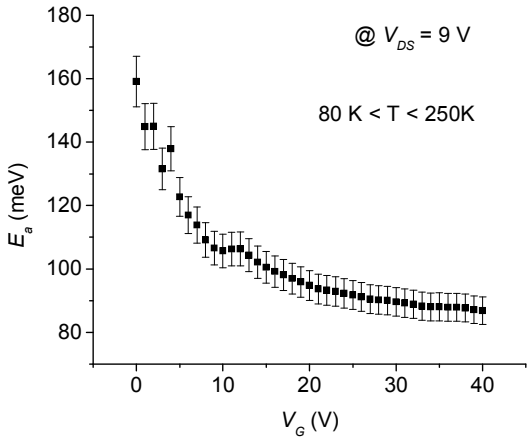


Fig. 3.6 Activation energy E_a vs. V_G at V_{DS} = 9 V (80 K < T < 250 K)

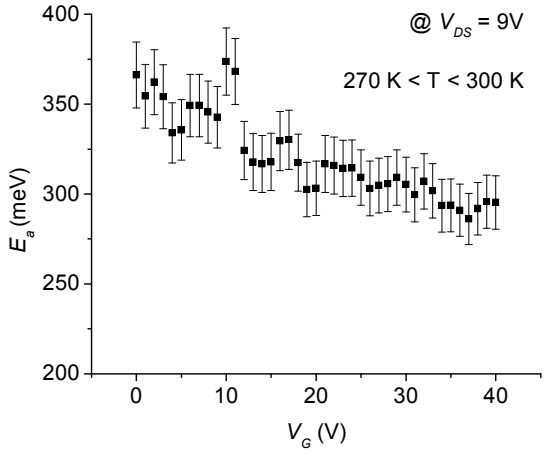


Fig. 3.7 Activation energy E_a vs. V_G at V_{DS} = 9 V (270 K < T < 300 K)

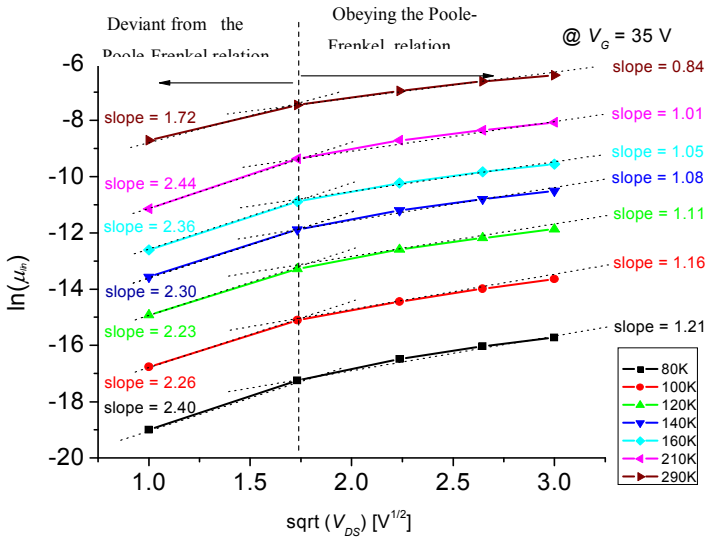
3.3.3.2 Field-dependent linear regime mobility

In order to check the dependence of mobility on the electric field induced by drain voltage, the Poole-Frenkel relation was applied [89,94]:

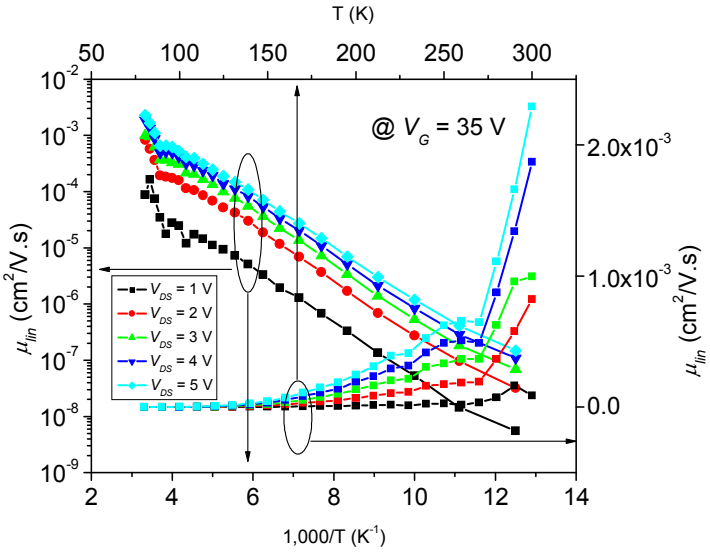
$$\mu(E) = \mu(0)\exp(\frac{q}{kT}\beta\sqrt{E}) = \mu(0)\exp(\sqrt{\frac{E}{E_o}}) \tag{3.8}$$

where $\mu(0)$ is the mobility at zero electric field, $\beta = (q/\pi\varepsilon\varepsilon_o)^{1/2}$ is the the Poole-Frenkel factor, $E_o = (\frac{kT}{q\beta})^2$, and E is the magnitude of the electric field.

If the average electric field ($E = V_{DS}/L$) is considered in the channel, and the mobility behavior follows the Poole-Frenkel relation, the slope of ln(μ) vs. $\sqrt{V_{DS}}$ is supposed to be unity. The linear regime mobility seems to obey the Poole-Frenkel relation quite well over the whole temperature range except for the case of very low drain voltage, e.g., V_{DS} = 1 V (Fig. 3.8) . It is believed that the low field effect mobility at very low drain voltage is due to the contact resistance at the interfaces between the source/drain electrodes and the PDI-8CN_2 channel.



(a) μ_{lin} vs. $\sqrt{V_{DS}}$ at $V_G = 35$ V



(b) ln(μ_{lin}) vs. 1/T and T at $V_G = 35$

Fig. 3.8 Field-dependent linear regime mobility: The linear regime mobility obeys the Poole-Frenkel relation quite well over the whole temperature range except for the case of very low drain voltage, e.g., $V_{DS} = 1$ V.

3.3.3.3 Saturation regime mobility

The saturation regime mobility μ_{sat} also exhibits the dependence on gate voltage and temperature at three distinct temperature regions, the same as those in the linear regime: 80 K < T < 250 K, 250 K < T < 270 K, and 270 K < T < 300 K (Fig. 3.9).

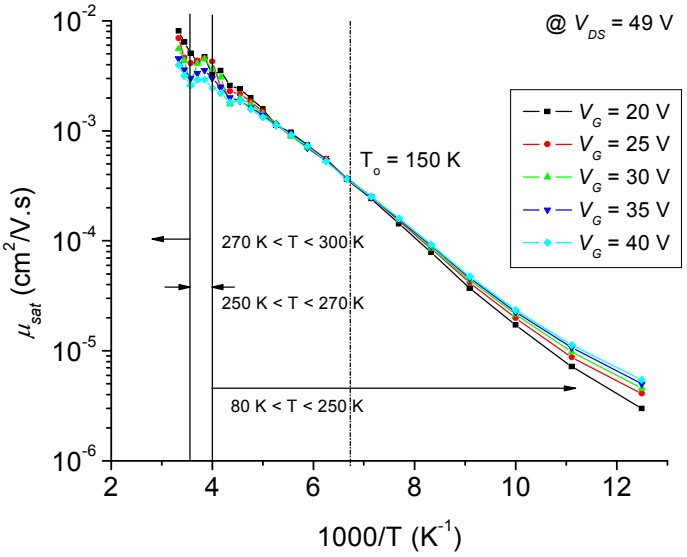


Fig. 3.9 Saturation regime mobility μ_{sat} vs. 1/T at V_{DS} = 49 V. The saturation regime mobility μ_{sat} also exhibits the dependence on gate voltage and temperature at three distinct temperature regions that are the same as those in the linear regime: 80 K < T < 250 K, 250 K < T < 270 K, and 270 K < T < 300 K.

In the case of the saturation regime, however, an isokinetic point is found at 150 K. Roughly speaking, the saturation regime mobility is higher than the linear regime mobility by an order of magnitude over the whole temperature range, which is attributable to the reduced contact resistance effect at higher drain voltages. This is also

explained by the reduced activation energy by 20 to 30 meV at 80 K < T < 250 K (Fig. 3.10) and 20 to150 meV at 270 K < T < 300 K (Fig. 3.11) compared to the linear regime. At the intermediate temperature region (250 K < T < 270 K), the activation energy is virtually zero, as is the case with the linear regime.

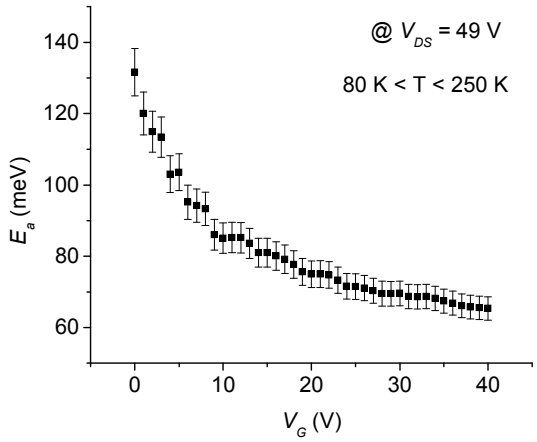


Fig. 3.10 Activation energy E_a vs. V_G at V_{DS} = 49 V (80 K < T < 260 K)

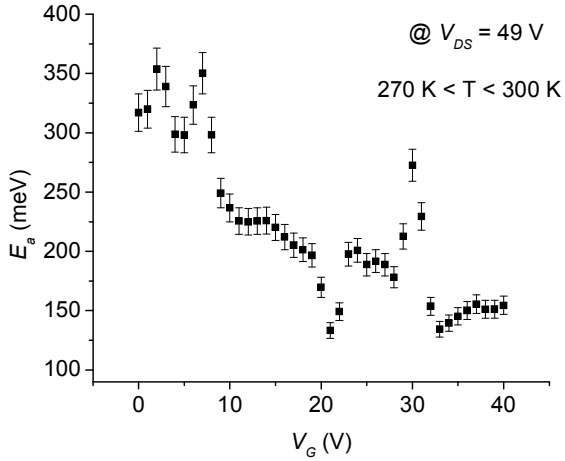


Fig. 3.11 Activation energy E_a vs. V_G at V_{DS} = 49 V (280 K < T < 300 K)

3.3.3.4 Field-dependent saturation regime mobility

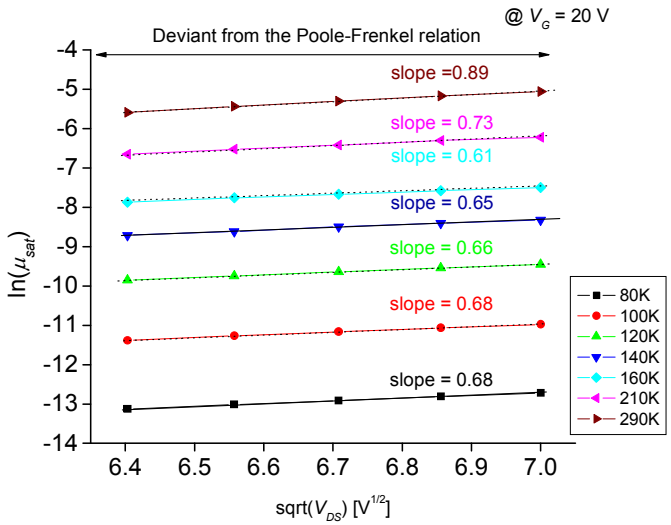
The dependence of saturation regime mobility on the lateral field is shown in Fig. 3.12. In general, as speculated from the output characteristics of OFETs, the saturation regime mobility is expected to be less drain-voltage-dependent than the linear regime mobility. Therefore, the $\ln(\mu_{sat})$ vs. $\sqrt{V_{DS}}$ plot is supposed to exhibit smaller slopes than $\ln(\mu_{lin})$ vs. $\sqrt{V_{DS}}$ fitting. Fig. 3.12 shows that the slopes are much smaller than expected by the Poole-Frenekel relation. Channel length modulation is the most probable mechanism to explain the slow increase in mobility with drain voltage in the saturation regime [15]. Considering the channel length modulation effect, the drain current in the saturation regime I_{DS} is given by

$$I_{DS} = \frac{W}{2L}\mu_{sat}C_i(V_G - V_T)^2(1+\lambda V_{DS}) \tag{3.9}$$

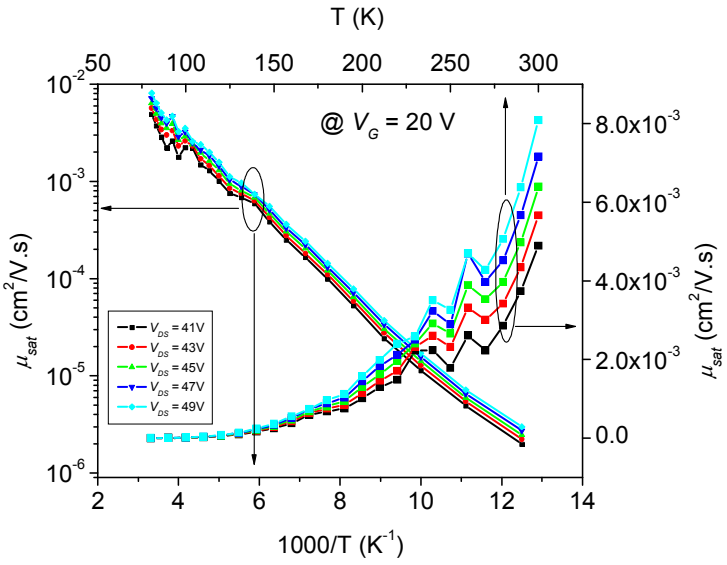
where the channel length modulation parameter λ relates the channel length pinch-off ΔL to drain voltage V_{DS} by

$$\frac{\Delta L}{L} = \lambda V_{DS} \tag{3.10}$$

Equation (3.10) implies that as the drain voltage increases, the effective channel length L - ΔL decreases, resulting in the increase in drain current and saturation mobility in equation (3.9).



(a) $\ln(\mu_{sat})$ vs. $\sqrt{V_{DS}}$ at $V_G = 20\text{V}$



(b) μ_{sat} vs. 1/T andT at $V_G = 20$ V

Fig. 3.12 Field-dependent saturation regime mobility. The saturation regime mobility is expected to be less drain-voltage-dependent than the linear regime mobility. Therefore, the $\ln(\mu_{sat})$ vs. $\sqrt{V_{DS}}$ plot is supposed to exhibit smaller slopes than the $\ln(\mu_{lin})$ vs. $\sqrt{V_{DS}}$ plot.

3.3.3.5 Trap density

By the combination of equations (3.3) and (3.6), the trap density is derived as a function of both gate voltage and Fermi-level over the temperature range 80 K to 300 K (Fig. 3.13, Fig. 3.14). In using equation (3.3), the adjustable parameter $\mu_0 N_c$ is found to be 10^{11}/V.s, which minimizes the scattering of the trap distribution calculated at various temperatures [Fig. 3.14 (b)]. Fig. 3.13 shows that the filled trap states exponentially increase with gate voltage as speculated from the MTR model.

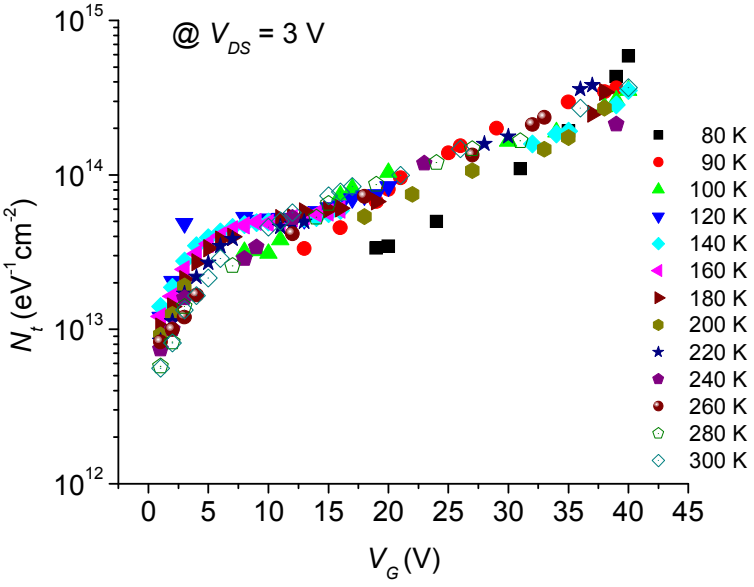
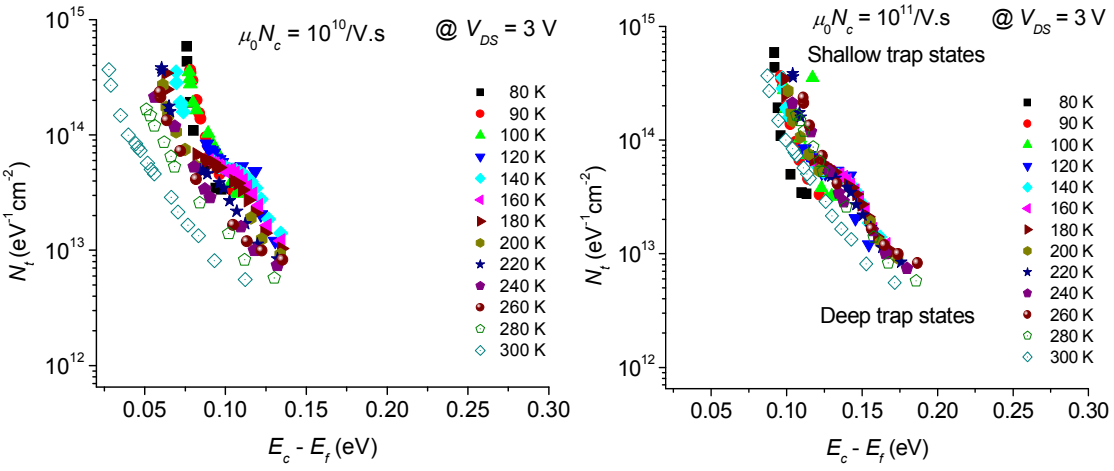
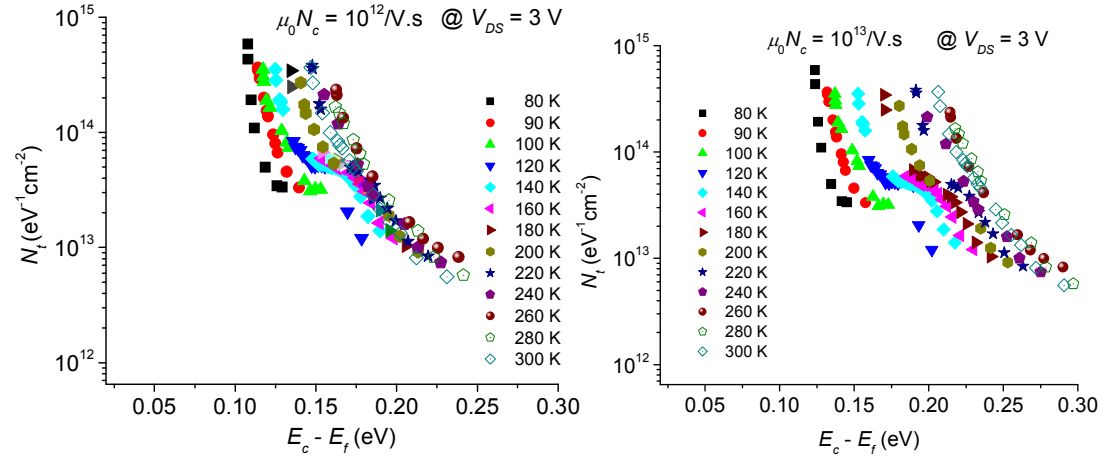


Fig. 3.13 Filled trap density N_t vs. V_G. The filled trap states exponentially increase with gate voltage as speculated from the MTR model.



(a) $\mu_o N_c = 10^{10}$/V.s

(b) $\mu_o N_c = 10^{11}$/V.s



(c) $\mu_o N_c = 10^{12}$/V.s

(d) $\mu_o N_c = 10^{13}$/V.s

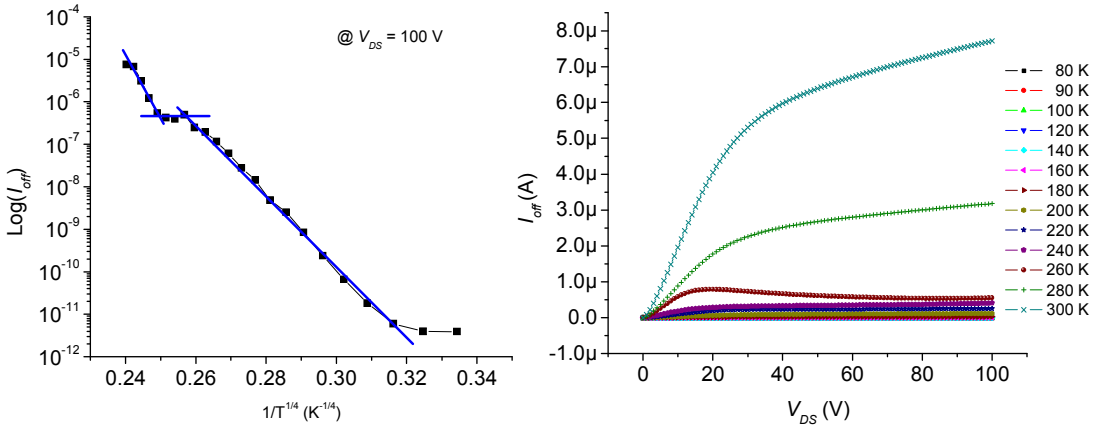
Fig. 3.14 Determination of the product $\mu_o N_c$ from N_t vs. E_c - E_f plots. The adjustable parameter $\mu_0 N_c$ is found to be (b) 10^{11}/V.s, which minimizes the scattering of the trap distribution calculated at various temperatures.

3.3.3.6 Off current

As shown in Fig. 3.15 (a), the off current as a function of temperature is locally consistent with Mott's variable range hopping (VRH) formula, which describes the dependence of conductivity and mobility on temperature for disordered materials [95,96]:

$$\sigma = \sigma_0 \exp\left[-\left(\frac{T_0}{T}\right)^{1/4}\right] \tag{3.11}$$

The temperature-independent off current between 230 K and 260 K is probably caused by the hygroscopic nature of HMDS molecules as previously explained in section 3.3.3.1. In this temperature region (230 K < T < 260 K), therefore, the off current does not increase with temperature because of the electron-trapping by the electronegative $(OH)^-$ groups.



(a) I_{off} vs. $1/T^{1/4}$ (b) I_{off} vs. V_{DS} and temperature

Fig. 3.15 Off-current behavior of the PDI-8CN_2 OFET. The off current as a function of temperature is locally consistent with Mott's variable range hopping (VRH) formula. The temperature-independent off current between 230 K and 260 K is probably caused by the hygroscopic nature of HMDS molecules.

3.4 Contact resistance in PDI-8CN_2 based OFETs

3.4.1 CONTACT RESISTANCE IN OFETS

Contact resistance phenomenon, which is brought about by the formation of Schottky barriers at the interfaces between the metal contacts and the source/drain wells, is relatively well understood in Si MOSFETs [72,97]. In OFETs, in the same way, contact resistance R_{SD}, which is the sum of source resistance R_S and drain resistance R_D, has its origin in the charge injection barriers at the interfaces between the source/drain electrodes and the organic semiconductor of interest. The injection barriers usually result from the poor ordering of semiconductor molecules; the poor molecular ordering is attributable to high surface tension of the metal electrodes [1,41-45,87]. In OFETs with relatively small device dimensions, contact resistance, compared to channel resistance, is so significant that it must be taken into consideration. In addition, the attempts to find intrinsic device parameters are obscured by the existence of contact resistance. Therefore, the analyses of contact resistance in OFETs are crucial to their practical applications.

There are three common techniques to measure the contact resistance in OFETs: four-probe measurement [25,82,98-100]; variable channel-length measurement [101-105]; and scanning Kelvin probe microscopy measurement (SKPM) [106-113]. Of the three techniques, the four-probe measurement has advantages over the other two methods in that it can be implemented using just one device and does not require high-cost scanning microscopy equipment. The basic idea of this technique is to place two sense probes between the source electrode and the drain electrode. Each of the two probes

makes up less than 10% of channel length and penetrates less than 10% of the channel width.

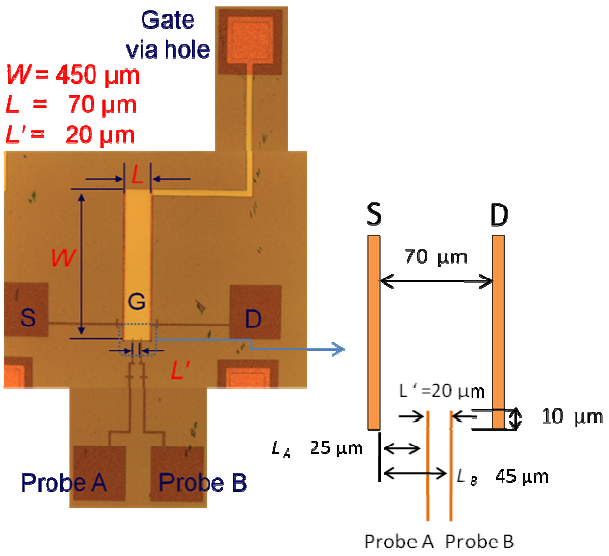
3.4.2 EXPERIMENTS

PDI-8CN_2 based bottom contact devices were fabricated on a Si substrate covered with a thick SiO_2 layer. The gate electrode was obtained from a highly phosphorus-doped LPCVD poly-Si layer of 4,000 Å that was patterned by conventional optical lithography. The gate dielectric consisted of a layer of 3,500 Å LTO (SiO_2). A bilayer deposition of 25 Å Ti / 450 Å Au was performed to form the source/drain electrodes and the two sense probes. The device fabrication process was completed with a thermal evaporation of PDI-8CN_2, during which the temperature of the substrate was kept at 100 ºC under a vacuum of 3×10^{-7} torr. The deposition rate was maintained at 0.1 ~ 0.2 Å/s up to an initial 60 Å, and increased to 0.6 ~ 0.7 Å/s for an additional 390 Å. The channel width W and the channel length L were 450 μm and 70 μm, respectively. The two sense probes were 3 μm in width and penetrated into the channel by 10 μm, forming a 20 μm spacing L' between them. The final device structure is shown in Fig. 3.16.

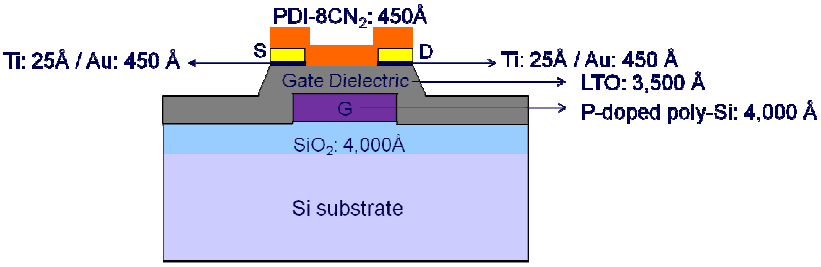
Variable temperature electrical measurements were performed under a vacuum less than 1×10^{-4} torr using liquid nitrogen as the coolant, where the temperature ranged from 130 K to 300 K with a step of 10 K.

In general, linear regime mobility is more sensitive to contact resistance than saturation regime mobility; that is, contact resistance is more likely to limit the drain current in the linear regime than in the saturation regime. This is because, at high gate voltages, the ratio of channel resistance to contact resistance decreases, so that the drain

current depends more heavily on contact resistance than on channel resistance [25]. Therefore, analyzing the linear regime characteristics suffices to understand the degree to which contact resistance affects the behavior of PDI-8CN$_2$ based OFETs.



(a) Top view



(b) Cross-section

Fig. 3.16 Device structure of the four-probe PDI-8CN$_2$ bottom contact device for contact resistance measurement. Two sense probes were 3 μm in width and penetrated into the channel by 10 μm, forming a 20 μm spacing *L'* between them.

3.4.3 RESULTS

3.4.3.1 Contact-corrected linear regime mobility

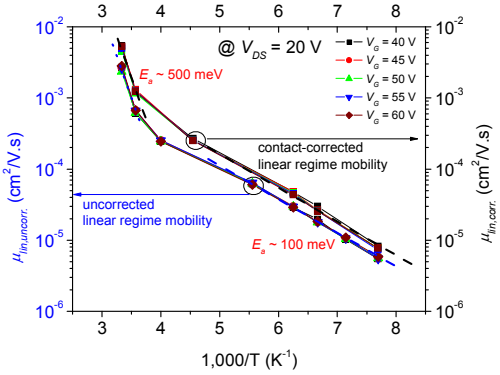
The contact-corrected linear regime mobility $\mu_{lin,corr.}$ is calculated by

$$\mu_{lin,corr.} = \left(\frac{\partial I_D}{\partial V_G} \right) \frac{L'}{WC_i(V_B - V_A)} \tag{3.12}$$

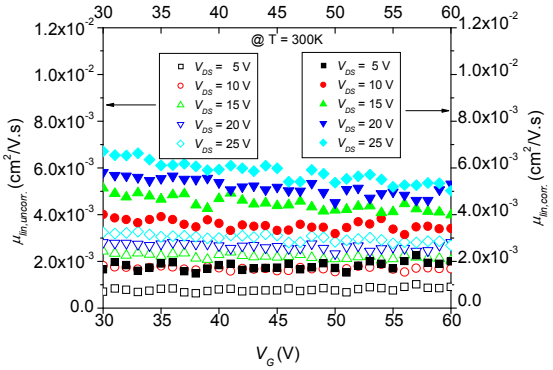
where V_A and V_B represent the voltages measured at the probe A and B. The capacitance of the LTO gate dielectric layer C_i is equal to 1.08×10^{-8} F/cm^2.

In Fig. 3.17, the contact-corrected and the uncorrected linear regime mobility are plotted as a function of (a) inversed temperature 1,000/T and (b) gate voltage V_G. The contact-corrected linear regime mobility is higher than the uncorrected linear regime mobility by a significant degree over the whole temperature range [Fig. 3.17 (a)]. It is also seen that the linear regime mobility increases by a factor of about two when the contact resistance effect is considered [Fig 3.17 (b)]. These results imply that the contact resistance has significant influences on the behavior of PDI-8CN$_2$ based OFETs, thereby bringing about the need for measuring its magnitude. Based on Fig. 3.17 (a), a few findings are worth commenting on the trap states of the device. First, the activation energy is independent of whether the mobility is contact-corrected or not, which means that the traps are phenomena most likely limited to the channel. Second, the two different activation energy values, 500 meV in the higher temperature region and 100 meV in the lower temperature region, hint at the existence of both deep and shallow traps. Finally, the linear regime mobility is a function of temperature only at gate voltages over $V_G = 40$ V, which signifies that most of the traps are filled at a certain gate voltage below 40 V.

The independence of the linear regime mobility of gate voltage is verified quite well in Fig. 3.17 (b).



(a) Contact-corrected and uncorrected linear regime mobility vs. 1/T at V_{DS} = 20 V



(b) Contact-corrected and uncorrected linear regime mobility vs. V_G at 300 K

Fig. 3.17 Contact-corrected and uncorrected linear regime mobility. (a) The contact-corrected linear regime mobility is higher than the uncorrected linear regime mobility by a significant degree over the whole temperature range. It is also seen that the linear regime mobility increases by a factor ~2 when the contact resistance effect is considered. The linear regime mobility is a function of temperature only at gate voltages over V_G = 40 V, which signifies that most of the traps are filled at a certain gate voltage below 40 V. (b) The independence of the linear regime mobility of gate voltage is verified quite well.

3.4.3.2 Contact resistance in linear regime

If a linear distribution of potential is assumed across the channel, the voltage drops at the source electrode ΔV_S and at the drain electrode ΔV_D can be determined by extrapolating the channel potential gradient to the source/drain electrodes (Fig. 3.18) [82]. The resulting ΔV_S and ΔV_D are given by equations (3.13.a) and (3.13.b):

$$\Delta V_s = [V_A - \frac{V_B - V_A}{L_B - L_A} \times L_A] \tag{3.13.a}$$

$$\Delta V_D = V_{DS} - [V_B + \frac{V_B - V_A}{L_B - L_A} \times (L - L_B)] \tag{3.13.b}$$

These voltage drops are the charge injection barriers resulting from the poor ordering of PDI-8CN_2 molecules on the source/drain metal electrodes.

Based on the measured sense probe potentials V_A, V_B and the drain current I_D, the channel resistance R_{SD} is expressed by

$$R_{SD} = R_S + R_D = \frac{\Delta V_S + \Delta V_D}{I_D} \tag{3.14}$$

In addition, the total resistance R_{tot}, which is the sum of the contact resistance R_{SD} and the channel resistance R_{ch}, is given by

$$R_{tot} = \frac{V_{DS}}{I_D} = R_{SD} + R_{ch} \tag{3.15}$$

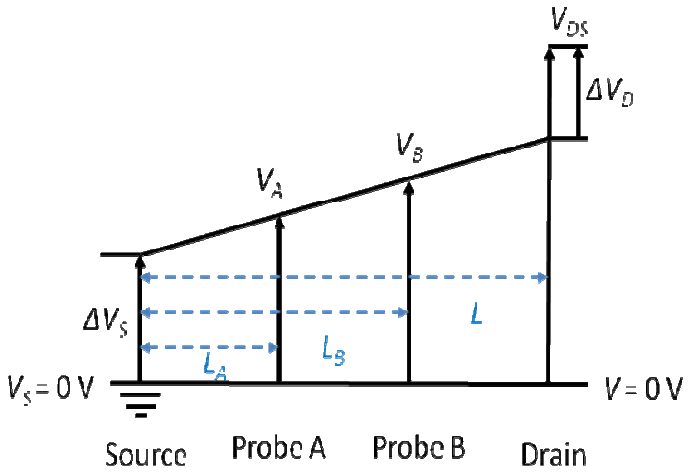
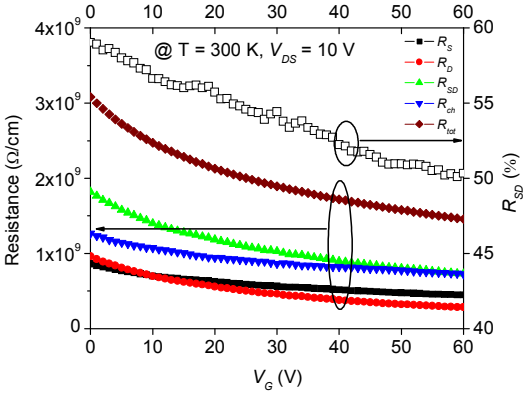


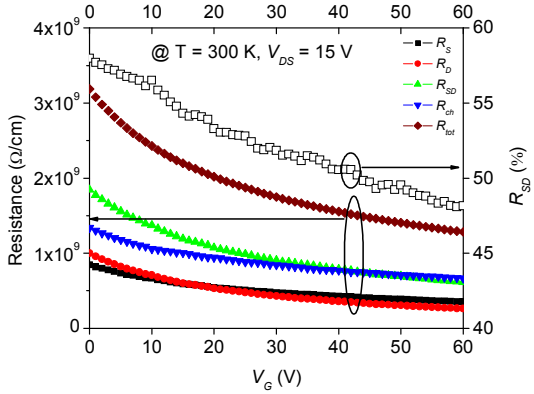
Fig. 3.18 Modeling of voltage drops at the source/drain electrodes. If a linear distribution of potential is assumed across the channel, the voltage drops at the source electrode ΔV_S and at the drain electrode ΔV_D can be determined by extrapolating the channel potential gradient to the source/drain electrodes. These voltage drops are the charge injection barriers resulting from the poor ordering of PDI-8CN$_2$ molecules on the source/drain metal electrodes; From [82].

The gate-voltage dependence of the resitance components (source reistance R_S; drain resistance R_D; contact resistance R_{SD}; channel resistance R_{ch}; and total resistance R_{tot}) is illustrated in Fig. 3.19 at T = 300 K and V_{DS} = 10 V, 15 V, 20 V, and 20 V. All the resistance components are nomalized with respect to the channel width 450 μm. The contact resistance percentage of total resistance is also presented in the same plots corresponding to each drain voltage. In all of the cases given, contact resitance turns out to be comparable to channel resistance, amounting to 45 to 60% of total resistance. Considering that the device has a relatively large channel length of 70 μm, contact

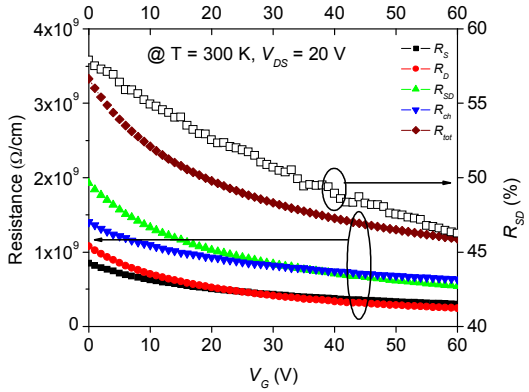
resistance is too substantial to be ignored. Moreover, contact resistance effects are expected to be much more significant for smaller channel devices.



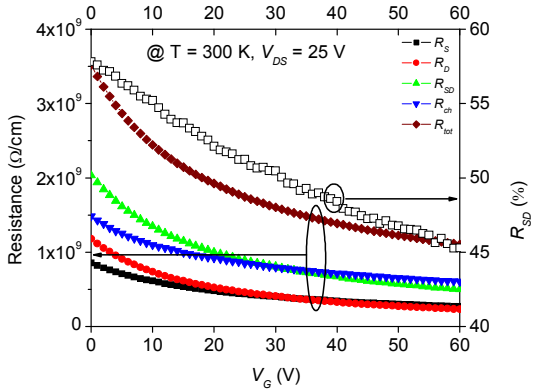
(a) At T = 300 K and V_{DS} = 10 V



(b) At T = 300 K and V_{DS} = 15 V



(c) At T = 300 K and V_{DS} = 20 V



(d) At T = 300 K and V_{DS} = 25 V

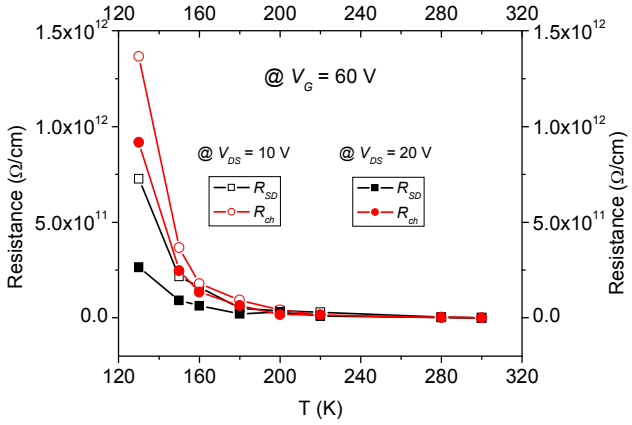
Fig. 3.19 Resistance components as a function of gate voltage at T = 300 K and V_{DS} = 10 V, 15 V, 20 V, and 25 V : 1) Contact resitance turns out to be comparable to channel resistance, amounting to 45 to 60% of total resistance. 2) Raised gate voltage results in lowered injection barriers in the contacts as well as facilitates charge tranport in the channel. 3) Drain resitance seems to be more sensitive to gate voltage change than source resistance because the channel deepening is the most conspicuous at the drain edge.

Both contact resistance and channel reistance decrease as gate voltage increases. In other words, raising gate voltage results in lowered injection barriers in the contacts as well as facilitates charge tranport in the channel. In the case of contact resitance, drain resitance seems to be more sensitive to gate voltage change than source resistance. This discrepancy can be explained as follows: The channel depth is different from point to point across the channel ; it is the deepest at the edge of the source electrode and the most shallow at the edge of the drain electrode. As gate volatge increases, the number of accumulated charges increases in the channel, deepening the channel. However, the channel deepening is the most conspicuous at the drain edge, whose net result is a relativley high decrease in drain resistance with increasing gate voltage. The decrease in channel resistance with increasing gate voltage is well understood in terms of the MTR model.

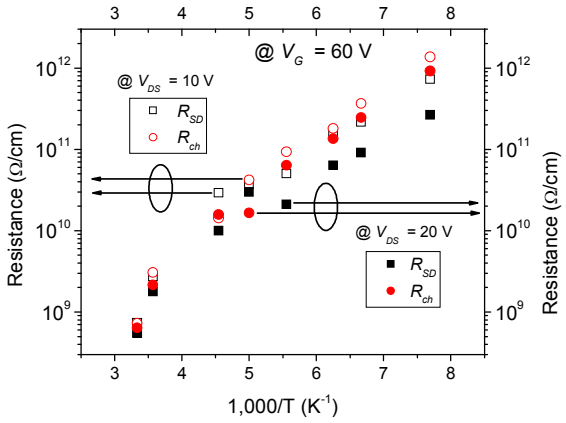
According to Fig. 3.19 (a) ~ (d), the percentage of total resistance accouting for contact resistance diminishes as drain voltage increases. Considering that the Poole-Frenkel relation implies that channel resistance also decreases with increasing drain voltage, contact resistance is more likely drain-voltage-dependent than channel resistance. Therefore, especially in the case of low drain voltage, contact resistance can act as a major charge injection barrer at the interfaces between the source/drain electrodes and the channel.

The dependence of contact resistance and channel resistance on temperarure is presented in Fig. 3.20. Under V_G = 60 V, the open squares and circles correspond to contact resistance and channel resistance, respectively, at V_{DS} = 10 V ; similarly, the solid

squares and circles represent contact resistance and channel resistance, respectively, at V_{DS} = 20 V. It is observed that both contact resistance and channel resistance decrease exponentially as temperature increases. This result agrees with the generally-accepted thermally-assisted charge transport phenomena in OFETs.



(a) Contact resistance vs. T



(b) Contact resistance vs. 1/T

Fig. 3.20 Contact resistance and channel resistance as a function of (a) T (a) and (b) 1/T at V_G = 60 V and V_{DS} = 10 V, 20 V. Both contact resistance and channel resistance decrease exponentially as temperature increases.

3.5 Conclusions

In order to make the best use of organic field-effect transistors (OFETs), the realization of organic complementary circuits is essential. To this end, *n*-channel organic semiconductors are as important as *p*-channel counterparts. Despite the significant progress in synthesizing new *n*-channel organic materials, their charge transport mechanisms are not understood as clearly as those of *p*-channel organic materials like pentacene. For that reason, as a stepping stone to establishing the suitable charge transport mechanisms in a relatively new air-stable *n*-channel material PDI-8CN_2 and related *n*-channel organic semiconductors, this chapter has dealt with the dependence of the electrical behavior on temperature and gate voltage as well as the effects of contact resistance in PDI-8CN_2 based OFETs.

First, based on the MTR model, relations such as the dependence of mobility on gate voltage and temperature, field-dependent mobility, trap density, and off current were derived in PDI-8CN_2 based OFETs. The dependence of linear regime mobility on gate voltage and temperature exhibited three distinct temperature domains: 80 K < T < 250 K; 250 K < T < 270 K; and 270 K < T < 300 K. At 80 K to 250 K, the linear regime mobility was dependent on temperature as well as gate voltage. In this temperature region, the activation energy E_a decreased as gate voltage increased with an isokinetic point at 250 K, which was explained by the MTR model. However, the linear regime mobility was nearly independent of gate voltage and temperature between 250 K and 270 K, which was characterized by virtually zero activation energy. This abnormal mobility behavior was explained with the trap-like electronegative hydroxyl $(OH)^-$ groups that result from

the hygroscopic nature of HMDS molecules. In the high temperature region (270 K < T < 300 K), the linear regime mobility was temperature-dependent, but very weakly gate-voltage-dependent. The existence of both deep and shallow trap states was inferred from the different activation energy values in the higher and lower temperature regions. The field-dependent linear regime mobility conformed to the Poole-Frenkel relation quite well over the whole temperature range with the exception of very low drain voltage. The low field effect mobility at very low drain voltage was due to the contact resistance. The saturation regime mobility also showed the dependence on gate voltage and temperature at three distinct temperature regions: 80 K < T < 250 K, 250 K < T < 270 K, and 270 K < T < 300 K, creating an isokinetic point at 150 K. Because of the reduced contact resistance effect, the saturation regime mobility was higher than that of the linear regime by approximately an order of magnitude over the whole temperature range. This was also explained by the reduced activation energy compared to the linear regime. At the intermediate temperature region (250 K < T < 270 K), the activation energy was virtually zero as was the case with the linear regime. Because of the lesser dependence of saturation mobility on drain voltage, the $\ln(\mu_{sat})$ vs. $\sqrt{V_{DS}}$ plot exhibited smaller slopes than the $\ln(\mu_{lin})$ vs. $\sqrt{V_{DS}}$ plotting. The trap density was derived as a function of both gate voltage and Fermi-level over the temperature range 80 K to 300 K. The filled trap states exponentially increased with gate voltage. The off current was locally consistent with Mott's variable range hopping (VRH) formula. The temperature-independent behavior in the temperature region 230 K to 260 K and the drastic surge in the off current above 260

K were explained by the hygroscopic nature of HMDS molecules, as was the case with mobility.

Second, using a four-probe measurement technique, contact-corrected linear regime mobility and contact resistance were calculated. The contact-corrected linear regime mobility was higher than the uncorrected linear regime mobility by a significant degree over the whole temperature range; for example, it was higher than the uncorrected linear regime mobility by approximately a factor of two at 300 K. This result brought about the need for measuring the magnitude of the contact resistance in PDI-8CN_2 based OFETs. Even in the case of a relatively large channel length of 70 μm, the contact resitance turned out to be comparable to channel resistance, amounting to 45 to 60% of total resistance. Both contact resistance and channel reistance decreased as gate voltage increased. In the case of contact resitance, drain resitance was more sensitive to gate voltage change than source resistance, which was explicable by the channel depth difference across the channel. The decrease in channel resistance with increasing gate voltage was explained by the MTR model. Since the Poole-Frenkel relation implies that channel resistance also decreases with increasing drain voltage, especially in the case of low drain voltage, contact resistance can act as a major charge injection barrer at the interfaces between the source/drain electrodes and the channel. It was observed that both contact resistance and channel resistance decrease exponentially as temperature increases. This result agrees with the generally-accepted thermally-assisted charge transport phenomena in OFETs.

CHAPTER 4 DUAL-CHANNEL ORGANIC FIELED-EFFECT TRANSISOTS

4.1 Introduction

Conventional organic field-effect transistors (OFETs) have three terminal electrodes: source, drain, and gate. The electrode materials include metals, highly-doped Si substrates, conducting polymers, and so on. In general, the three-terminal OFETs are inherently capable of exhibiting unipolar behavior. In other words, they are categorized into either hole-transporting or electron-transporting OFETs, depending on the type of the channel material; in some cases, through the use of particular gate dielectrics, ambipolar behavior is observed in some organic semiconductors [57]. Therefore, in order to obtain *p*-channel and *n*-channel FETs, two separate fabrication processes are usually required.

Four-terminal geometry is a unique way of achieving a dual-channel device in a single fabrication process. In previous work, this technique was successfully employed to realize a Si-organic hybrid dual-channel MOSFET, in which a Si *n*-channel and an organic *p*-channel were coupled with each other [114]. Even though these hybrid four-terminal devices proved to be effective in organic vapor sensing, they were inevitably accompanied by high cost and high temperature Si processes such as ion implantation, annealing, thermal oxidation, etc.

This chapter discusses the realization of nearly all organic dual-channel devices. Basically, these devices are four-terminal OFETs that consist of a stack of bottom metal

Source1/Drain1 electrodes, a polymeric *p*-type organic semiconductor layer, a polymeric gate dielectric, a small molecule *n*-type organic semiconductor layer, and top metal Source2/Drain2 electrodes. In the resultant device configuration, the polymeric *p*-channel and the small molecule *n*-channel are coupled with each other. Thermally-evaporated Au layers were used to form the bottom and top source/drain electrodes. The device fabrication procedure required no high cost or high temperature processes except for the thermal evaporation for the Au layers and the *n*-channel layer.

These dual-channel organic devices are promising in that they are applicable to chemically sensitive organic vapor sensors. In essence, because both of their gates and channels are made up of organic semiconductors, the dual-channel chemical sensors can be operated in both the organic FET (OFET) mode [115,116] and the insulated gate FET (IGFET) mode [117,118], which provides them with a wide range of chemical detection. Additionally, these sensor devices can be operated in a "chemical memory" mode [1].

4.2 Experiments

4.2.1 DEVICE FABRICATION

Dual-channel organic FETs were fabricated on a Si substrate covered with a 1,000 Å thick SiO_2 insulating layer. Poly-3-hexylthiophene (P3HT), PDI-8CN_2, and a new polymeric Merck® dielectric (DS121) were used as the *p*-channel material, the *n*-channel material, and the gate dielectric, respectively.

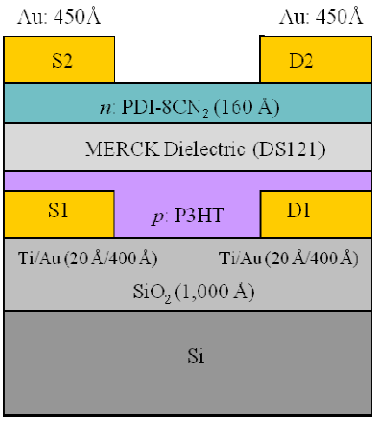


Fig. 4.1 Structure of the dual-channel organic device with W = 15,000 μm, L = 100 μm; P3HT, PDI-8CN_2, and a polymeric dielectric (DS121) were used as the *p*-channel material, the *n*-channel material, and the gate dielectric, respectively. The two channels are coupled with each other.

The schematic of the dual-channel organic FET is shown in Fig. 4.1. Initially, a bilayer of Ti/Au (20 Å/400 Å) was thermally evaporated onto the Si substrate through a shadow mask with channel length W = 15,000 μm and channel width L = 100 μm, to form the source (S1) and drain electrodes (D1) of the *p*-channel field-effect transistor (*p*-FET). A P3HT solution of 1.3 wt. % concentration was prepared using chloroform ($CHCl_3$) as the solvent, and subsequently spin-cast on the Si-substrate for 30 sec. at 3,000 rpm. Next,

the as-supplied Merck® dielectric (DS121) was spin-cast on the P3HT layer for 45 sec. at 3,500 rpm followed by a 15 min. curing at 140 ºC; under such spin conditions, the dielectric thickness was found to be 2 μm. Both the P3HT and DS121 castings were performed under a nitrogen (N_2) environment. The device fabrication process was carried on with the sublimation of PDI-8CN_2 (160 Å) under a vacuum of 3×10^{-7} torr, keeping the substrate temperature at 100 ºC. The deposition rate was maintained at 0.1 ~ 0.2 Å/s for an initial 60 Å, and then increased to 0.4 ~ 0.5 Å for an additional 100 Å. Device fabrication was completed with thermal evaporation of Au (450 Å), using the shadow mask with W = 15,000 μm and L = 100 μm, to form the source (S2) and drain electrodes (D2) of the *n*-channel field-effect transistor (*n*-FET).

4.2.2 ORGANIC VAPOR SENSING

In order to confirm the usefulness of the dual-channel organic FET as an organic vapor-detecting sensor, two analyte sources were used: isopropyl alcohol (IPA, C_3H_8O) and ethanol (C_2H_5OH). The analytes were delivered to an operating dual-channel device using a peristaltic pump; the analyte delivery started at t = 60 s and ended at t = 80 s. The response to the analytes was determined by the change in the drain current during the analyte delivery. The dual-channel device was operated in both *p*-FET and *n*-FET modes, which makes it possible to evaluate the selectivity difference between the two modes. For the convenience of comparison, the drain current change was normalized with respect to its value at t = 10 s.

4.3 Analyses of the device characteristics

The equilibrium energy-level alignment in the dual-channel device is shown in Fig. 4.2. While the Fermi level of P3HT is known to locate at the position 0.7 eV above its HOMO level, the Fermi level of PDI-8CN$_2$ has not been determined [119,120]. However, in thermal equilibrium, the Fermi level is constant for the P3HT, DS121, PDI-8CN$_2$ layers. Considering that the operating voltages are very high for both the *p*-FET and the *n*-FET compared to their energy band-gaps, the band bending due to the work function difference between P3HT and PDI-8CN$_2$ is thought to be negligible.

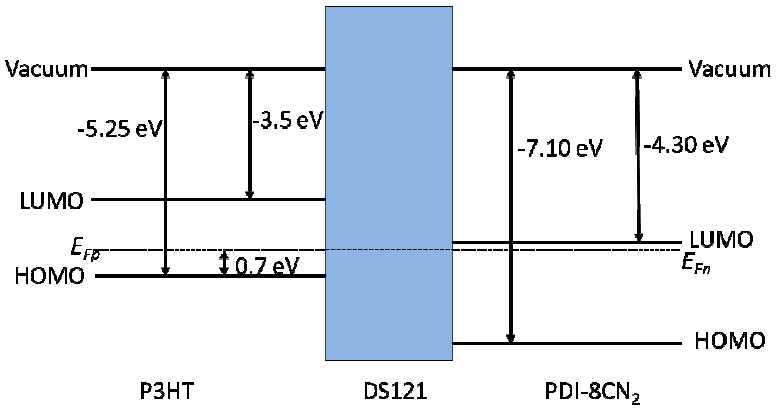


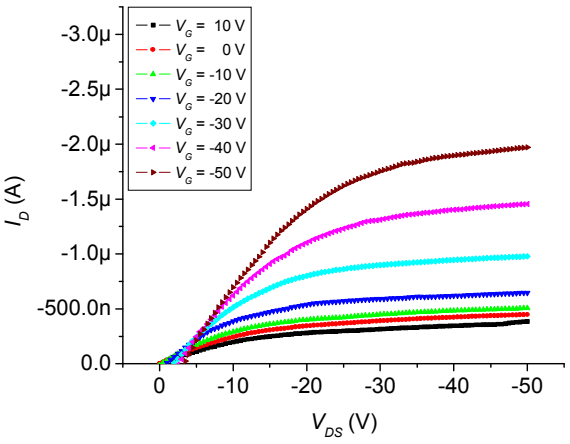
Fig. 4.2 Energy-level alignment between P3HT and PDI-8CN$_2$ in thermal equilibrium; the operating voltages for both the *p*-FET and the *n*-FET are high enough to negate the band bending due to their work function difference.

In the case of the *p*-FET operation, the two upper electrodes (S2, D2) are under the same negative potential, or a gate voltage of $V_G = V_{S2S1} = V_{D2S1}$ with respect to the lower electrode (S1). This potential distribution raises the Fermi level for PDI-8CN$_2$ from

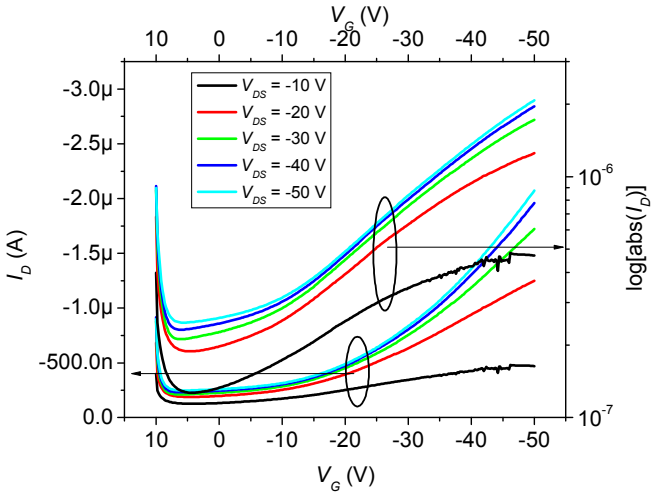
E_{Fn} to $E_{Fn} + q\,|\,V_G\,|$, which will induce a band bending of P3HT and accumulate positive carriers (holes) at its surface. These accumulated holes are charge carriers for the drain current in the *p*-FET.

By contrast, in the case of the *n*-FET operation, the two lower electrodes (S1, D1) are under the same positive potential, or a gate voltage of $V_G = V_{S1S2} = V_{D1S2}$ with respect to the upper electrode (S2). This positive potential lowers the Fermi level for P3HT from E_{Fp} to $E_{Fp} - q\,|\,V_G\,|$. The lowered Fermi level is accompanied by a band bending of PDI-$8CN_2$ at its surface, accumulating negative charge carriers (electrons) at its surface. These accumulated electrons are charge carriers for the drain current in the *n*-FET.

Fig. 4.3 presents (a) the output characteristics and (b) the transfer characteristics of the *p*-FET. In addition, (a) the output characteristics and (b) the transfer characteristics of the *n*-FET are shown in Fig. 4.4. Both the *p*-FET and the *n*-FET exhibit decent output characteristics at $|\,V_{DS}\,| \leq 50$ V and $|\,V_G\,| \leq 50$ V with the exception of the high off current in the *p*-FET. Because the off current is very low in the *n*-FET, the high off current in the *p*-FET seems to result from the intrinsic properties of the P3HT layer, which is confirmed by the positive threshold voltage of 19.7 V. The relatively high gate leakage current is believed to be reduced by optimizing the parameters for gate dielectric (DS121) casting such as spin speed and time, curing temperature and time, etc. From a high frequency CV measurement at 1 MHz, the capacitance of the DS121 layer was calculated to be 1.5 nF/cm^2, yielding the saturation mobility of 3.7×10^{-3} cm^2/V.s for the *p*-FET and 1.5×10^{-2} cm^2/V.s for the *n*-FET. The device characteristics of the *p*-FET and the *n*-FET are summed up in Table 4.1.

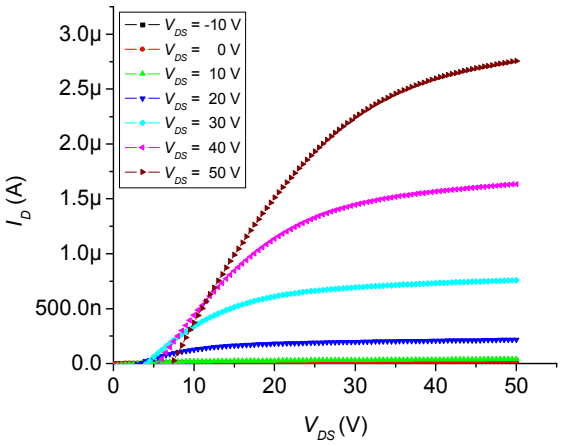


(a) Output charactersitics of the *p*-FET

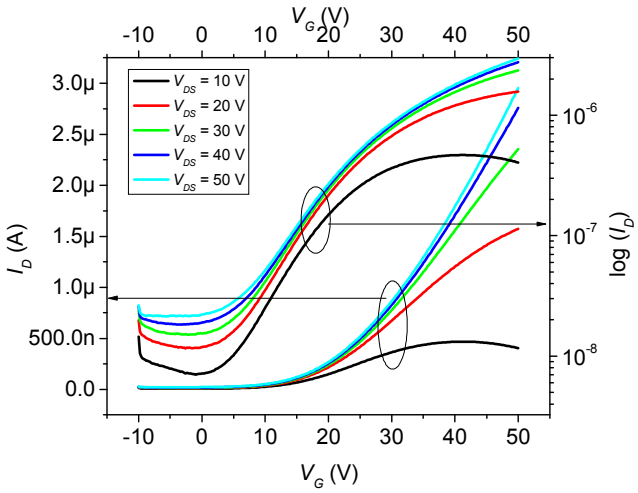


(b) Transfer charactersitics of the *p*-FET

Fig. 4.3 (a) Output characteristics and (b) transfer characteristics of the *p*-FET in the organic dual-channel device at $V_{DS} \leq$ -50 V and $V_G \leq$ -50 V.



(a) Output charactersitics of the *n*-FET



(b) Transfer charactersitics of the *n*-FET

Fig. 4.4 (a) Output characteristics and (b) transfer characteristics of the *n*-FET in the organic dual-channel device at $V_{DS} \leq 50$ V and $V_G \leq 50$ V.

	p-FET	*n*-FET
$\mu_{sat.}$ (cm^2/V.s)	3.7×10^{-3}	1.5×10^{-2}
V_T (V)	19.7	8.2
I_{on}/I_{off}	4.4×10^{0}	1.4×10^{2}

Table 4.1 Device characteristics of the *p*-FET and the *n*-FET in the dual-channel OFET. Both the *p*-FET and the *n*-FET exhibit decent output characteristics at $\left| V_{DS} \right| \leq 50$ V and $\left| V_G \right| \leq 50$ V with the exception of the high off current in the *p*-FET. Because the off current is very low in the *n*-FET, the high off current in the *p*-FET seems to result from the intrinsic properties of the P3HT layer, which is confirmed by the positive threshold voltage of 19.7 V.

4.4 Organic chemical sensing using the dual-channel OFETs

In terms of organic vapor sensing modes, the *p*-FET can be considered as a sensing gate field-effect transistor (SGFET) with the PDI-8CN_2 thin film as its gate electrode as well as sensing layer (Fig. 4.1) [117,118]. If the same negative potential is applied to the two upper metal electrodes (S2,D2) with respect to the lower electrode (S1), the whole PDI-8CN_2 thin film functions as the gate electrode of the *p*-FET. The introduction of organic analytes will modify the work function, i.e., the Fermi level for the PDI-8CN_2. This work function modification is accompanied by the change in the charge density in the *p*-channel (P3HT). The net result is the increase or decrease in the drain current of the *p*-FET. Meanwhile, the *n*-FET can be regarded as an organic field-effect transistor (OFET) sensor. Under the same positive potential to the lower electrodes (S1,D1) with respect to the upper electrode (S2), the PDI-8CN_2 thin film functions as both the channel material and the sensing layer. Introduced analytes will change the induced charge density in the *n*-channel depending on the analyte types, thereby altering the drain current of the *n*-FET. While trap-like analytes will reduce the charge density, dopant-like anaytes will increase the charge density.

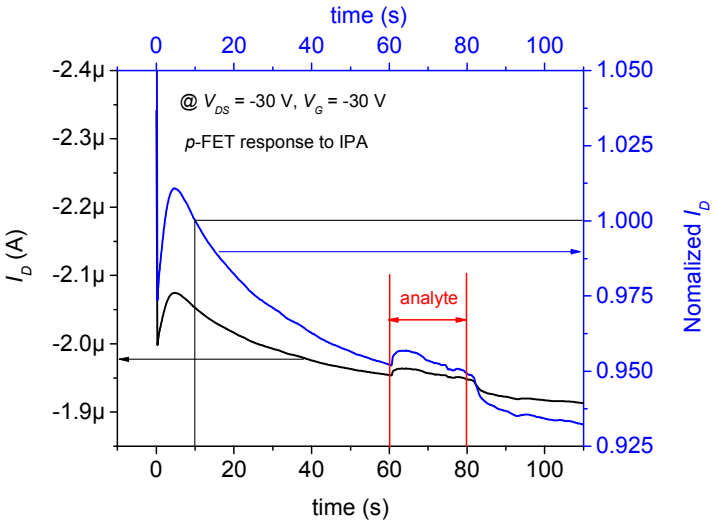
The responses of the *p*-FET and the *n*-FET to IPA and ethanol vapors are shown in Fig. 4.5 and Fig. 4.6, respectively. The *p*-FET was operated at V_{D1S1} = -30 V and V_G = V_{S2S1} = V_{D2S1} = -30 V, and the *n*-FET was operated at V_{D2S2} = 40 V and V_G = V_{S1S2} = V_{D1D2} = 40 V. In each of the plots, the left axis Y represents the drain currents at a certain time, and the right axis Y represents the normalized drain current with respect to its value at t =

10s. The start (at t = 60 s) and the end (at t = 80 s) of the analyte delivery are marked in red. For each case, the sensitivity (%) was expressed by:

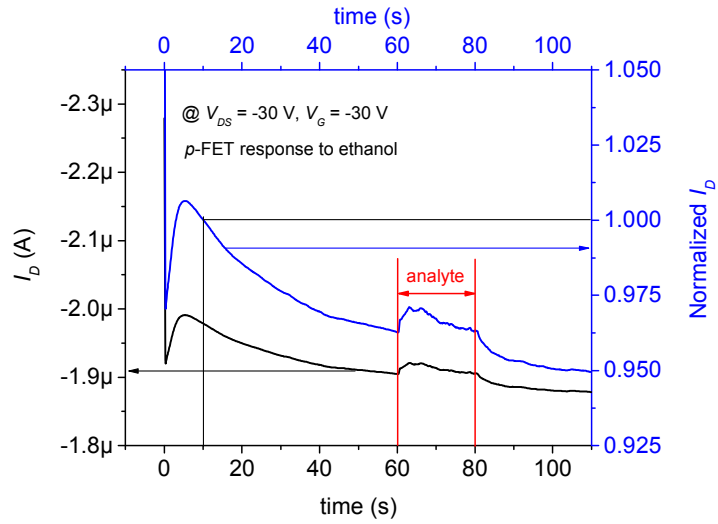
$$\text{sensitivity}(\%) = \left|\frac{I_{D,\text{max}} - I_{D,\text{t=60 s}}}{I_{D,\text{t=60 s}}}\right| \times 100 \quad (4.1)$$

where $I_{D,\text{t=60s}}$ is the drain current at t = 60 s and $I_{D,\text{max}}$ is the maximum drain current during the analyte delivery.

Upon being exposed to IPA and ethanol vapors, both the *p*-FET and the *n*-FET exhibit the increases in drain current. However, there is a remarkable difference in the drain current behavior between the FET sensors; while the increase in drain current is temporary in the *p*-FET, the drain current of the *n*-FET increases continuously during the analyte delivery. The resulting sensitivity of the *p*-FET is 0.4% for IPA and 0.8% for ethanol, whereas that of the *n*-FET is 6% for IPA and 9% for ethanol. Table 4.2 summarizes the responses to IPA and ethanol vapors in the *p*-FET and *n*-FET sensing modes.

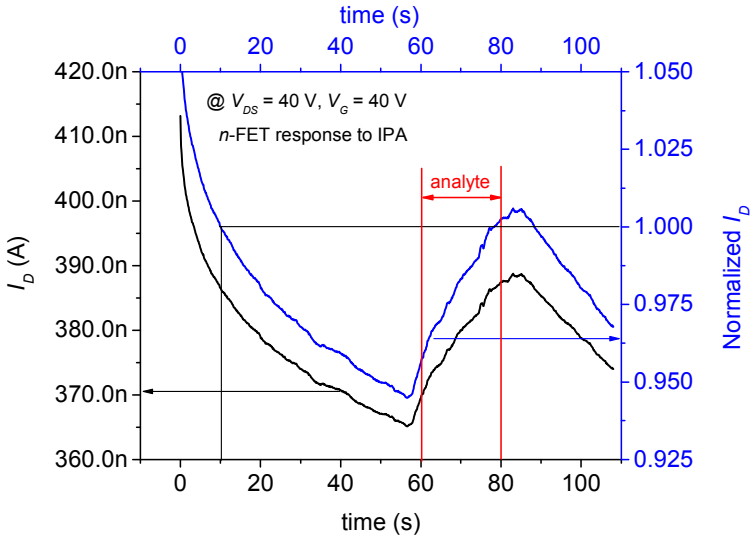


(a) Response of the *p*-FET to the IPA vapor

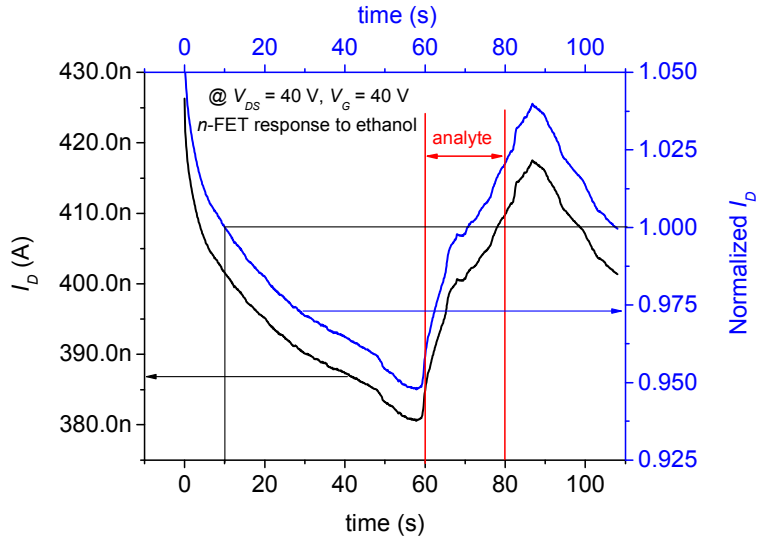


(b) Response of the *p*-FET to the ethanol vapor

Fig. 4.5 Responses of the *p*-FET to (a) the IPA vapor and (b) the ethanol vapor. The *p*-FET was operated at V_{D1S1} = -30 V and $V_G = V_{S2S1} = V_{D2S1}$ = -30 V. The left axis Y represents the drain currents at a certain time, and the right axis Y represents the normalized drain current with respect to its value at t = 10 s. The start (at t = 60 s) and the end (at t = 80 s) of the analyte delivery are marked in red.



(a) Response of the *n*-FET to the IPA vapor



(b) Response of the *n*-FET to the ethanol vapor

Fig. 4.6 Responses of the *n*-FET to (a) the IPA vapor and (b) the ethanol vapor. The *n*-FET was operated at V_{D2S2} = 40 V and $V_G = V_{S1S2} = V_{D1D2}$ = 40 V. The left axis Y represents the drain currents at a certain time, and the right axis Y represents the normalized drain current with respect to its value at t = 10 s. The start (at t = 60 s) and the end (at t = 80 s) of the analyte delivery are marked in red.

			p-FET	*n*-FET
Chemical sensing mode			Sensing gate FET (SGFET)	Organic FET (OFET)
Sensitivity (%)	Analytes	IPA	0.4	6
		ethanol	0.8	9
Relative sensitivity			Lower	Higher

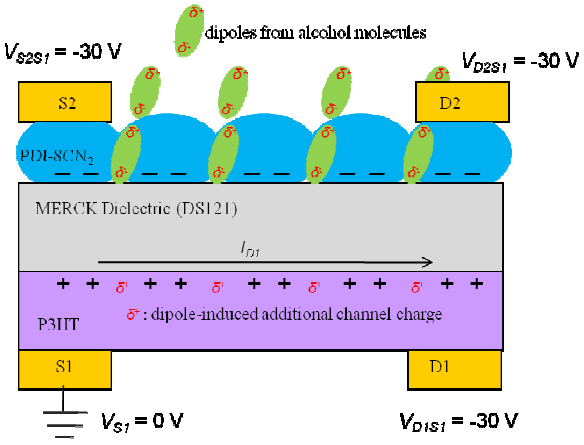
Table 4.2 Comparison of sensitivity to the IPA and ethanol vapors between the *p*-FET and the *n*-FET. The sensitivity difference between the *p*-FET mode and the *n*-FET mode is understandable in terms of the bias-stress effect combined with the changed channel charge density induced by the dipoles of the alcohol molecules. In the *p*-FET mode, the bias-stress effect is more dominant in deciding the drain current than the dipole effect. In contrast, the dipole effect is a more dominant factor in deciding the drain current in the *n*-FET mode than the bias-stress effect. The sensitivity difference to the IPA vapor and the ethanol vapor results from the dipole moment difference between their molecules.

The increases in drain current in the *p*-FET and the *n*-FET are explainable in terms of the dipole moments of the alcohol molecules (Fig. 4.7). Because of the polar hydroxyl group[$(OH)^-$], alcohols are polar compounds that have partial positive charges (δ^+) on carbon and hydrogen, and a partial negative charge (δ^-) on oxygen; the partial

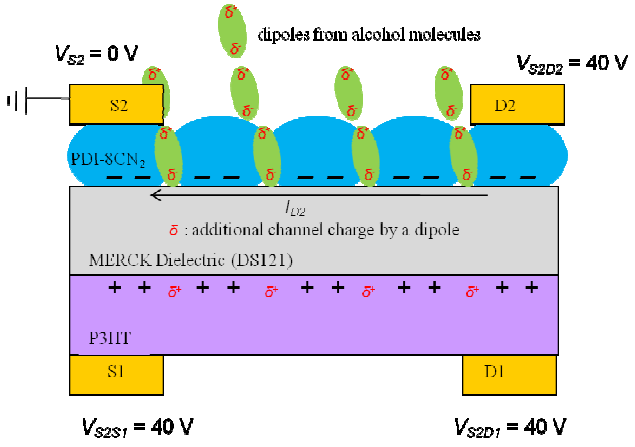
positive and negative charges have the same magnitude (δ) as each other [16]. This partial charge distribution brings about the dipole moment μ given by

$$\mu = \delta \times d \tag{4.2}$$

where d is the distance between the partial positive and negative charges. The dipole moment is expressed in D (debye); one debye is equal to 3.34×10^{-30} C.m. The dipole moments of gas-state IPA and ethanol are 1.66 D and 1.69 D, respectively. The increased drain current in the p-FET results from the additional channel charge carriers (δ^+) that are induced by the dipole moment of the alcohol molecules [Fig. 4.7 (a)]. The alcohol molecules are supposed to migrate through the grain boundaries of the PDI-8CN_2 layer because the grain boundaries consist of relatively open spaces compared to the bulk PDI-8CN_2. Considering the potential distribution in Fig. 4.7 (a), the dipoles of the alcohol molecules will align nearly perpendicularly to the interface between the PDI-8CN_2 layer and the gate dielectric (DS121). The partial negative charges (δ^-) of the dipoles face the interface and induce the dipole-induced additional positive charges (δ^+) to the p-channel. As a result of the dipole-induced positive charges, the drain current I_{D1} increases. The increase in drain current in the n-FET arises from the additional n-channel charges (δ^-) by the dipoles of the alcohol molecules [Fig. 4.7 (b)]. These negative partial charges induce an equal amount of positive charges (δ^+) to the P3HT layer that acts as the gate electrode of the n-FET. Consequently, the drain current I_{D2} in the n-FET increases as a result of the interaction between the partial negative charges (δ^-) and the induced positive charges (δ^+).



(a) Drain current increase in the *p*-FET



(b) Drain current increase in the *n*-FET

Fig. 4.7 Mechanisms showing the drain current increase with the introduction of the alcohol molecules in (a) the *p*-FET and (b) the *n*-FET. The increased drain current in the p-FET results from the additional channel charge carriers (δ^+) that are induced by the dipole moment of the alcohol molecules. The increase in drain current in the *n*-FET arises from the additional *n*-channel charges (δ^-) by the dipoles of the alcohol molecules.

The remarkable sensitivity difference between the *p*-FET and the *n*-FET sensing modes is understandable in terms of the bias-stress effect combined with the change in the channel charges induced by the dipoles. In the *p*-FET mode, the drain current initially increases with the introduction of the alcohol analytes, but decreases with the increase in time even during the analyte delivery. The decreasing drain current with time means that the channel charges, the sum of the field-induced and dipole induced charges, undergo the bias-stress effect. The bias-stress effect seems to play a more dominant role in deciding the drain current in the *p*-FET mode sensing than the dipole effect by the alcohol molecules. In contrast, the drain current in the *n*-FET mode continuously increases with time during the analyte delivery. Because the PDI-8CN_2 layer is exposed to the delivered anaytes, the channel current in the *n*-FET is directly influenced by the partial negative charges (δ^-) of the dipoles. The dipole effect seems to be more dominant in deciding the drain current in the *n*-FET than the bias-stress effect.

Even though it is not obvious, the sensitivity difference to the IPA vapor and the ethanol vapor is likely due to their vapor pressure difference; e.g., 33 mmHg for IPA and 44.6 mmHg for ethanol at 20 ºC. Under a certain environment, more ethanol molecules are expected to slide to the PDI-8CN_2 layer than IPA molecules. Therefore, the ethanol vapor is expected to yield a higher sensitivity than the IPA vapor.

4.5 Conclusions

Nearly all organic dual-channel devices were realized. Basically, theses devices are a four-terminal OFET with P3HT, PDI-8CN_2, and a polymeric Merck® dielectric (DS121) as the *p*-channel material, the *n*-channel material, and the gate dielectric, respectively. In the resultant device configuration, the polymeric *p*-channel and the small molecule *n*-channel are coupled with each other.

In terms of device characteristics, both the *p*-FET and the *n*-FET exhibited decent output characteristics at $|V_{DS}| \leq 50$ V and $|V_G| \leq 50$ V. The device performances of the *p*-FET and the *n*-FET were comparable to each other. The *p*-FET showed a saturation mobility of 3.7×10^{-3} cm^2/V.s, a threshold voltage of 19.7 V, and an I_{on}/I_{off} ratio of 4.4×10^0. In the *n*-FET, the saturation mobility was 1.5×10^{-2} cm^2/V.s, the threshold voltage was 8.2 V, and the I_{on}/I_{off} ratio was 1.4×10^2. Because the off current was very low in the *n*-FET, the high off current in the *p*-FET probably resulted from the intrinsic properties of the P3HT layer, which was consistent with the positive threshold voltage of 19.7 V. The relatively high gate leakage current of the dual-channel devices is believed to be reduced by optimizing the parameters for gate dielectric (DS121) casting.

In order to check its viability as an organic vapor sensor, the dual-channel organic FET was operated under the introduction of the IPA and ethanol vapors as the analytes. Exposed to the IPA and ethanol vapors, both the *p*-FET and the *n*-FET exhibited an increased drain current. The resulting sensitivity of the *p*-FET mode was 0.4% for IPA and 0.8% for ethanol. In the *n*-FET mode, the resultant sensitivity was 6% for IPA and 9% for ethanol. The remarkable sensitivity difference between the *p*-FET mode and the

n-FET mode was explicable in terms of the bias-stress effect combined with the changed channel charge density induced by the dipoles of the alcohol molecules. In the *p*-FET mode, the drain current initially increased with the analytes of the alcohols, but decreased with time even during the analyte delivery; the bias-stress effect played a more dominant role in deciding the drain current in the *p*-FET mode than the dipole effect by the alcohol molecules. In contrast, the drain current in the *n*-FET mode continuously increased with time during the anlayte delivery. Considering that the PDI-8CN_2 layer was exposed to the delivered analytes, the dipole effect was a more dominant factor in deciding the drain current in the *n*-FET mode than the bias-stress effect. The different sensitivities to the IPA vapor and the ethanol vapor probably resulted from the vapor pressure difference between them. With the relatively higher vapor pressure, the ethanol vapor is expected to exhibit a higher sensitivity than the IPA vapor.

CHAPTER 5 CONCLUSIONS

This work has dealt with three subtopics: Pentacene-based low voltage *p*-channel OFETs with anodized gate dielectrics; Charge transport in PDI-8CN_2 based *n*-channel OFETs; and Dual-channel OFETs.

Pentacene-based low voltage top-contact *p*-channel OFETs were realized using three different anodized gate dielectrics: a 470 Å SiO_2, a 1,700 Å Ta_2O_5, and an 800 Å Ta_2O_5 obtained from an *n*-Si wafer, a sputtered Ta layer, and an e-beam evaporated Ta layer, respectively. First, the anodization of the *n*-Si wafer formed a 470 Å SiO_2 layer with an RMS surface roughness of 4.6 Å and a capacitance of 140 nF/cm^2. The device with the anodized SiO_2 gate dielectric, exhibited a saturation mobility of 0.38 cm^2/V.s, a threshold voltage of -0.01 V, and an I_{on}/I_{off} ratio of 3.4×10^1 at $V_{DS} \leq$ -10 V and gate voltage $V_G \leq$ -4 V. An OTS treatment on the SiO_2 surface improved the saturation mobility to 0.88 cm^2/V.s, and the I_{on}/I_{off} ratio to 2.3×10^2, along with a 93% reduction in the gate leakage current (from -11 nA to -800 pA at V_{DS} = 0 V and V_G = -4 V). The threshold voltage was increased by -1.01 V from the OTS treatment. The improved saturation mobility was consistent with the larger grain size of pentacene in the OTS-treated device. The improved I_{on}/I_{off} ratio and the reduced gate leakage current were based on the nature of the OTS SAM as a coating layer that reduces the interface component of the total off current as well as prevents charge carriers from tunneling through the relatively leaky anodized SiO_2 gate dielectric. The increased threshold voltage arose from

the substantial capacitance of the OTS SAM. Second, the 1,700 Å anodized Ta_2O_5, which was obtained from the sputtered Ta thin film, exhibited a relatively poor RMS surface roughness of 22.9 Å and a capacitance of 270 nF/cm^2. Using the 1,700 Å anodized Ta_2O_5 as the gate dielectric, the device with the saturation mobility of 0.52 cm^2/V.s, the linear region mobility of 0.22 cm^2/V.s at V_{DS} = -5 V and V_G = -3 V, the threshold voltage of -1.28 V, and the I_{on}/I_{off} ratio of 1.64×10^2 at $V_{DS} \leq$ -5 V and gate voltage $V_G \leq$ -2.5 V, was achieved. However, the device exhibited quite high gate leakage current that was nearly equal to one-tenth the drain current at V_{DS} = -5 V and V_G = -2.5 V. The problem of the relatively high gate leakage current was considerably reduced by 40% from an HMDS treatment and by 74% from an MDP treatment on the Ta_2O_5. The two surface treatments also resulted in the increased mobility values along with the improved I_{on}/I_{off} ratios by an order of magnitude, which means that both the HMDS treatment and the MDP treatment are effective in ordering pentacene molecules as well as coating the pentacene-Ta_2O_5 interface. The difference in threshold-voltage change after the two surface treatments is explainable by the relative molecular length difference between the two molecules; because of its shorter molecular length, the capacitance of the HMDS SAM is negligible compared to that of the MDP SAM. Consequently, the threshold voltage of the HMDS-treated device decreased by -0.75 V as a result of the larger grains of pentacene, which have fewer charge-carrier traps than the smaller grains. However, the threshold voltage of the MDP-treated device increased by -0.83 V due to the significant capacitance of the MDP SAM arising from its relatively long chain length. Finally, two batches of pentacene-based OFETs were fabricated using the 800 Å Ta_2O_5 as the gate

dielectric ($C_{Ta_2O_5}$ = 325 nF/cm^2) prepared by anodizing the e-beam evaporated Ta layer. The first batch consisted of a set of untreated and HMDS-treated devices and the second batch consisted of a set of untreated and MDP-treated devices. Both of the batches of devices showed reasonable output and transfer characteristics at $V_{DS} \leq$ -10V and $V_G \leq$ -5 V. The HMDS treatment changed the saturation mobility from 0.45 to 0.51 cm^2/V.s, the linear region mobility from 0.34 to 0.36 cm^2/V.s at V_{DS} = -3 V and V_G = -3 V, the threshold voltage from 0.56 to 1.96 V, and the I_{on}/I_{off} ratio from 7.5 × 10^1 to 1.2 × 10^1. The effects of the HMDS treatment were explainable with the same reasoning as that of the anodized Ta_2O_5 obtained from the sputtered Ta layer with the exception of the I_{on}/I_{off} ratio. The relatively poor I_{on}/I_{off} ratio resulted from the pentacene not being purified by sublimation. Indeed, in other experiments with the same gate dielectric and purified pentacene, I_{on}/I_{off} ratios over 10^4 were attained. In calculating the mobility values, if the capacitance of the HMDS SAM (C_{HMDS} = 1,000 nF/cm^2) was considered, the corresponding saturation and linear region mobility were 0.67 cm^2/V.s and 0.48 cm^2/V.s, respectively. These results imply that each mobility value can increase by more than 40% with the HMDS treatment. The MDP treatment altered the saturation mobility from 6.6 × 10^{-2} to 6.7 × 10^{-2} cm^2/V.s, the threshold voltage from 0.18 to -0.89 V, and the I_{on}/I_{off} ratio from 4.3 × 10^2 to 3.7 × 10^4. However, with the consideration of the capacitance of the MDP SAM (C_{MDP} = 900 nF/cm^2), the saturation mobility increased by a factor of 1.34. The effects of the MDP treatment were also explicable with the same reasoning as that of the anodized Ta_2O_5 obtained from the sputtered Ta layer.

In order to establish the suitable charge transport mechanisms in a relatively new air-stable *n*-channel material PDI-8CN_2 and related *n*-channel organic semiconductors, the dependence of the electrical behavior on temperature and gate voltage as well as the effects of contact resistance were studied in PDI-8CN_2 based OFETs. First, using the MTR model, relations such as the dependence of mobility on gate voltage and temperature, field-dependent mobility, trap density, and off current were derived. The dependence of linear regime mobility on gate voltage and temperature exhibited three distinct temperature domains: 80 K < T < 250 K; 250 K < T < 270 K; and 270 K < T < 300 K. At 80 K to 250 K, the linear regime mobility was dependent on temperature as well as gate voltage, which was explained by the MTR model. The linear region mobility that was nearly independent of gate voltage and temperature between 250 K and 270 K, was understood in terms of the trap-like electronegative hydroxyl $(OH)^-$ groups that resulted from the hygroscopic nature of HMDS molecules. In the high temperature region (270 K < T < 300 K), the linear regime mobility was temperature-dependent, but very weakly gate-voltage-dependent. The existence of both deep and shallow trap states was inferred from the different activation energy values in the higher and lower temperature regions. The field-dependent linear regime mobility was consistent with the Poole-Frenkel relation over the whole temperature range except for very low drain voltage; the low field effect mobility at very low drain voltage was due to the contact resistance of the devices. The saturation regime mobility also showed the dependence on gate voltage and temperature at the three same distinct temperature regions as the linear regime. Due to the reduced contact resistance effect, the saturation regime mobility was higher than that of

the linear regime by an order of magnitude over the whole temperature range. The lesser dependence of saturation mobility on drain voltage provided the ln(μ_{sat}) vs. $\sqrt{V_{DS}}$ plot with smaller slopes than the ln(μ_{lin}) vs. $\sqrt{V_{DS}}$ plot. As for the trap density, the filled trap states exponentially increased with gate voltage. The off current locally obeyed Mott's variable range hopping (VRH) formula. The temperature-independent behavior in the temperature region 230 K to 260 K and the drastic surge in the off current above 260 K were explained by the hygroscopic nature of HMDS molecules, as was the case with the mobility. Second, contact-corrected linear regime mobility and contact resistance were calculated using a four-probe measurement technique. The contact-corrected linear regime mobility was higher than the uncorrected linear regime mobility by a significant degree over the whole temperature range. Even in the case of a relatively large channel length of 70 μm, the contact resitance amounted to 45 to 60% of the total resistance. Both contact resistance and channel reistance decreased as gate voltage increased. In the case of contact resitance, drain resitance was more sensitive to gate voltage change than source resistance due to the channel depth difference across the channel. The decrease in channel resistance with increasing gate voltage was explained by the MTR model. Because the Poole-Frenkel relation implies that channel resistance also decreases with increasing drain voltage, especially in the case of low drain voltage, contact resistance can act as a major charge injection barrer at the interfaces between the source/drain electrodes and the channel. It was observable that both contact resistance and channel resistance decreased exponentially as temperature increased, which agrees with the generally-accepted thermally-assisted charge transport phenomena in OFETs.

Nearly all organic dual-channel devices were realized using P3HT, PDI-8CN_2, and a polymeric dielectric as the *p*-channel material, the *n*-channel material, and the gate dielectric, respectively. In these dual-channel devices, the *p*-channel and the *n*-channel were coupled with each other. Both the *p*-FET and the *n*-FET exhibited decent output characteristics at $|V_{DS}| \leq 50$ V and $|V_G| \leq 50$ V. The *p*-FET showed a saturation mobility of 3.7×10^{-3} cm^2/V.s, a threshold voltage of 19.7 V, and an I_{on}/I_{off} ratio of 4.4×10^0. In the *n*-FET, the saturation mobility was 1.5×10^{-2} cm^2/V.s, the threshold voltage was 8.2 V, and the I_{on}/I_{off} ratio was 1.4×10^2. The high off current in the *p*-FET probably resulted from the intrinsic properties of the P3HT layer. The relatively high gate leakage current is believed to be reduced by optimizing the parameters for gate dielectric casting. As for organic vapor sensing, both the *p*-FET and the *n*-FET exhibited increased drain current when they were exposed to IPA and ethanol vapor. The sensitivity of the *p*-FET mode was 0.4% for IPA and 0.8% for ethanol and that of the *n*-FET mode was 6% for IPA and 9% for ethanol. The remarkable sensitivity difference between the *p*-FET mode and the *n*-FET mode was understandable in terms of the bias-stress effect combined with the changed channel charge density induced by the dipoles of the alcohol molecules. In the *p*-FET mode, the bias-stress effect played a more dominant role in deciding the drain current than the dipole effect by the alcohol molecules. In contrast, the dipole effect was a more dominant factor in deciding the drain current in the *n*-FET mode than the bias-stress effect. The different sensitivities to the IPA vapor and the ethanol vapor probably resulted from their vapor pressure difference.

Bibliography

[1] C. D. Dimitrakopoulos and P. R. Malenfant, Adv. Mater. 14, 99 (2002)

[2] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, Nature 403, 521 (2000)

[3] L. Wang, D. Fine, T. Jung, D. Basu, H. von Seggern, and A. Dodabalapur, Appl. Phys. Lett. 85, 1772 (2004)

[4] M. A. Baldo, M. E. Thompson, and S. R. Forrest, Nature 403, 750 (2000)

[5] M. A. Baldo, D. F. O'Brien, Y. You, A. Shoustikov, S. Sibley, M. E. Thompson, and S. R. Forrest, Nature 395, 151 (1998)

[6] C. Adachi, M. A. Baldo, S. R. Forrest, M. E. Thompson, Appl. Phys. Lett. 77, 904 (2000)

[7] C. J. Brabec, N. S. Sariciftci, and J. C. Hummelen, Adv. Funct. Mater. 11, 15 (2001)

[8] W. U. Huynh, J. J. Dittmer, A. P. Alivisatos, Science 295, 2425 (2002)

[9] P. Peumans, S. Uchida, and S. R. Forrest, Nature 425, 158 (2003)

[10] M. D. McGehee and A. J. Heeger, Adv. Mater. 12, 1655 (2000)

[11] A. Dodabalapur, M. Berggren, R. E. Slusher, Z. Bao, A. Timko, P. Schiortino, E. Laskowski, H. E. Katz, and O. Nalamasu, IEEE J. of Selected Topics in Quantum Electronics 4, 67 (1998)

[12] J. L. Brédas, J. Cornil, D. Beljonne, D. A. D. Santos, and Z. Shuai, Acc. Chem. Res. 32, 267 (1999)

[13] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, and D. M. de Leeuw, Nature 401, 685 (1999)

[14] A. J. Heeger, Rev. Mod. Phys. 73, 681 (2000)

[15] B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 5th Ed., Prentice Hall, Upper Saddle River, New Jersey (2000)

[16] W. H. Brown and C. S. Foote, Organic Chemistry, 3th Ed., Brooks/Cole, (2002)

[17] J. L. Brédas, J. P. Calbert, D. A. da Silva Filho, and J. Cornil, PNAS 99, 5804 (2002)

[18] G. Horowitz, R. Hajlaoui, R. Bourguiga, and M. Hajlaoui, Synth. Met., 101, 401 (1999)

[19] M. Malagoli and J. L. Brédas, Chem. Phys. Lett. 327, 13 (2000)

[20] K. Sakanoue, M. Motoda, M. Sugimoto, and S. Sakaki, J. Phys. Chem. A 103, 5551 (1999)

[21] J. Cornil, J. Ph. Calbert, and J. L. Brédas, J. Am. Chem. Soc. 123, 1250 (2001)

[22] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, IEEE Elect. Dev. Lett. 18, 87 (1997)

[23] C. R. Newman, C. D. Frisbie, D. A. da Silva Filho, J. L. Brédas, P. C. Ewbank, and K. R. Mann, Chem. Mater. 16, 4436 (2004)

[24] B. A. Jones, M. J. Ahrens, M. H. Yoon, A. Facchetti, T. J. Marks, and M. R. Wasielewski, Angew. Chem. Int. 43, 6363 (2004)

[25] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. da Silva Filho, J. L. Brédas, L. L. Miller, K. R. Mann, and C. D. Frisbie, J. Phys. Chem. B 108, 19281 (2004)

[26] B. Yoo, T. Jung, D. Basu, A. Dodabalapur, B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, Appl. Phys. Lett. 88, 082104 (2006)

[27] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3th ed., Wiley-Interscience, Hoboken, New Jersey (2007)

[28] J. Plummer, M. Deal, and P. Griffin, Prentice Hall, Upper Saddle River, New Jersey (2000)

[29] H. Y. Choi, S. H. Kim, and J. Jang, Adv. Mater. 16, 732 (2004)

[30] J. Lee, D. K. Hwang, J. M. Choi, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, Appl. Phys. Lett. 87, 023504 (2005)

[31] T. Jung, A. Dodabalapur R. Wenz, and S. Mohapatra, Appl. Phys. Lett. 87, 182109 (2005)

[32] J. Z. Wang, Z. H. Zheng, and H. Sirringhaus, Appl. Phys. Lett. 89, 083513 (2006)

[33] K. D. Kim and C. K. Song, Appl. Phys. Lett. 88, 233508 (2006)

[34] T. Maeda, H. Kato, and H. Kawakami, Appl. Phys. Lett. 89, 123508 (2006)

[35] J. Tate, J. A. Rogers, C. D. W. Jones, B. Vyas, D. W. Murphy, W. Li, Z. Bao, R. E. Slusher, A. Dodabalapur, and H. E. Katz, Langmuir 16, 6054 (2000)

[36] S. A. DiBenedetto, I. Paci, A. Facchetti, T. J. Marks, and M. A. Ratner, J. Phys. Chem. B 110, 22394 (2006)

[37] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, Nature 445, 745 (2007)

[38] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, Appl. Phys. Lett. 76, 1941 (2000)

[39] Y. D. Park, D. H. Kim, Y. Jang, M. Hwang, J. A. Lim, and K. Cho, Appl. Phys. Lett. 87, 243509 (2005)

[40] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, IEEE Transactions on Electron Devices 48, 1060 (2001)

[41] B. de Boer, H. Meng, D. F. Perepichka, J. Zheng, M. M. Frank, Y. J. Chabal, and Z. Bao, Langmuir 19, 4272 (2003)

[42] J. C. Love, L. A. Estroff, J. K. Kriebel, R. G. Nuzzo, and G. M. Whitesides, Chem. Rev. 105, 1103 (2005)

[43] P. Stoliar, R. Kshirsagar, M. Massi, P. Annibale, C. Albonetti, D. M. de Leeuw, and F. Biscarini, J. Am. Chem. Soc. 129, 6477 (2007)

[44] H. B. Akkerman, P. W. Blom, D. M. de Leeuw, and B. de Boer, Nature 441, 69 (2006)

[45] D. J. Gundlach, L. L. Jia, and T. N. Jackson, IEEE Elect. Dev. Lett. 22, 571 (2001)

[46] W. H. Kim, A. J. Mäkinen, N. Nikolov. R. Shashidhar, H. Kim, and Z. H. Kafafi, App. Phys. Lett. 80, 3844 (2002)

[47] S. Kirchmeyer and K. Reuter, J. Mater. Chem. 15, 2077 (2005)

[48] D. Chirvase, Z. Chiguvare, M. Knipper, J. Parisi, V. Dyakonov, and J. C. Hummelen, J. Appl. Phys. 93, 3376 (2003)

[49] P. Anderson, R. Forchheimer, P. Tehrani, and M. Berggren, Adv. Funct. Mater. 17, 3074 (2007)

[50] H. Rost, J. Ficker, J. S. Alonso, L. Leenders, and I. McCulloch, Synth. Met. 145, 83 (2004)

[51] A. Ulman, Chem, Rev. 96, 1533 (1996)

[52] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, Nat. Mater. 3, 317 (2004)

[53] D. J. Gundlach, H. Klauk, C. D. Sheraw, C. C. Kuo, J. R. Huang, and T. N. Jackson, IEDM 99, 111 (1999)

[54] A. Salleo, M. L. Chabinyc, M. S. Yang, and R. A. Street, Appl. Phys. Lett. 81, 4383 (2002)

[55] A. Dodabalapur, L. Torsi, and H. E. Katz, Science 268, 270 (1995)

[56] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y. Y. Lin, and A. Dodabalapur, Nature 404, 478 (2000)

[57] L. L. Chua, J. Zaumseil, J. F. Chang, E. C. W. Ou, P. K. H. Ho, H. Sirringhaus, and R. H. Friend, Nature 434, 194 (2005)

[58] A. Dodabalapur, Nature 434, 151 (2005)

[59] P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Graham, A. Curioni, and W. Andreoni, Appl. Phys. Lett. 80, 2517 (2002)

[60] A. Babel, S. A. Jenekhe, J. Am. Chem. Soc. 125, 13656 (2003)

[61] J. A. Letizia, A. Facchetti, C. L. Stern, M. A. Ratner, and T. J. Marks, J. Am. Chem. Soc. 127, 13476 (2005)

[62] B. K. Crone, A. Dodabalapur, R. Sarpenshkar, R. W. Filas, Y.-Y. Lin, Z. Bao, J. H. O'Neill, W. Li, and H. E. Katz, J. Appl. Phys. 89, 5125 (2001)

[63] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, Appl. Phys. Lett. 88, 083502 (2006)

[64] P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, and S. D. Theiss, Appl. Phys. Lett. 82, 3964 (2003)

[65] G. H. Gelinck, H. E. A. Huitema, E. Van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. Van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B.

Giesbers, B.-H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. Van Rens, and D. M. de Leeuw, Nat. Mater. 3, 106 (2004)

[66] L. Torsi and A. Dodabalpur, Anal. Chem. 77, 380A (2005)

[67] R. Rotzoll, S. Mohapatra, V. Olariu, R. Wenz, M. Grigas, K. Dimmler, O. Shchekin, and A. Dodabalapur, Appl. Phys. Lett. 88, 123502 (2006)

[68] T. Hori, Gate Dielectrics and MOS ULSIs (Springer, 1997)

[69] C. Bartic, H. Jansen, A. Campitelli, and S. Borghs, Org. Electron. 3, 65 (2002)

[70] K. W. Kwon, C. S. Kang, S.O. Park, H. K. Kang, and S. T. Ahn, IEEE Trans. Electron Device 43, 919 (1996)

[71] X. Wang and D. L. Kwong, IEEE Trans. Electron Device 53, 78 (2006)

[72] S. K. Ghandhi, VLSI Fabricaion Principles (Silicon and Gallium Arsenide), 2nd Ed., Wiley-Interscience, New York, NY (1994)

[73] Y. T. Jeong and A. Dodabalapur, Appl. Phys. Lett. 91, 193509 (2007)

[74] S. D. Ross, M. Finkelstein, and E. F. Rudd, Anodic Oxidation, Academic Press, Inc., New York, New York 1975)

[75] Y. Wang and M. Lieberman, Langmuir 19, 1159 (2003)

[76] I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S.Tierney, R,. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee, and M. F. Toney, Nat. Mater. 5, 328 (2006)

[77] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwase, Appl. Phys. Lett. 82, 4581 (2003)

[78] M. Textor, L. Ruiz, R. Hofer, A. Rossi, K. Feldman, G. Hähner, and N. D. Spencer, Langmuir 16, 3257 (2000)

[79] R. Hofer, M. Textor, and N. D. Spencer, Langmuir 17, 4014 (2001)

[80] M. J. O'Neil, A. Smith, and P. E. Heckelman, The Merck Index, 13th Ed., Merck, Rahway, New Jersey (2001)

[81] ACROS Organics: Catalog of Organics and Fine Chemicals, Fisher Scientific (2002/2003)

[82] R. J. Chesterfield, J. C. McKeen, C. R. Newman, C. D. Frisbie, P. C. Ewbank, K. R. Mann, and L. L. J. Appl. Phys. 95, 6396 (2004)
[83] P. G. Le Comber and W. E. Spear, Phys. Rev. Lett. 25, 509 (1970)
[84] M. Shur and M. Hack, J. Appl. Phys. 55, 3831 (1984)
[85] R. A. Street, Hydrogenated Amorphous Silicon, Cambridge University Press (1991)
[86] G. Horowitz, R. Hajlaoui, D. Fichou, and A. El Kassmi, J. Appl. Phys. 85, 3202 (1999)
[87] G. Horowitz, M. E. Hajlaoui, and R. Hajlaoui, J. Appl. Phys. 87, 4456 (2000)
[88] G. Horowitz, R. Hajlaoui, and P. Delannoy, J. Phys. III France 5, 355 (1995)
[89] G. Horowitz, Adv. Mater. 10, 365 (1998)
[90] C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, Science 283, 822 (1999)
[91] W. Brutting, Physic of Organic Semiconductors, WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany (2005)
[92] R. C. Haddon, T. Siegrist, R. M. Fleming, P. M. Bridenbaugh, and R. A. Laudise, J. Mater. Chem. 5, 1719 (1995)
[93] D. Suhl, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 13, 940 (1990)
[94] J. Frenkel, Phys. Rev. 54, 647 (1938)
[95] G. Paasch, T. Lindner, and S. Scheinert, Synth. Met. 132, 97 (2002)
[96] M.C.J.M. Vissenberg and M. Matters, Phys. Rev. B 57, 12964 (1998)
[97] S. Y. Chou and D. A. Antoniadis, IEEE Transactions on Electron Devices 34, 448 (1987)
[98] C. Chen and J. Kanicki, IEEE Electron. Dev. Lett. 18, 340 (1997)
[99] J. A. Merlo and C. D. Frisbie, J. Polym. Sci. B 41, 2674 (2003)
[100] V. Podzorov, V. M. Pudalov, and M. E. Gershenson, Appl. Phys. Lett. 82, 1739 (2003)
[101] R. A. Street and A. Salleo, Appl. Phys. Lett. 81, 2887 (2002)

[102] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols, and T. J. Jackson, Solid-state Electron. 47, 297 (2003)
[103] P. V. Necliudov, M. S. Shur, D. J. Gundlach, and T. J. Jackson, Solid-state Electron. 47, 259 (2003)
[104] M. Lefenfeld, G. Blanchet, and J. A. Rogers, Adv. Mater. 15, 1188 (2003)
[105] J. Zaumseil, K. W. Baldwin, and J. A. Rogers, J. Appl. Phys. 93, 6117 (2003)
[106] P. Annibale, C. Albonetti, P. Stoliar, and F. Biscarini, J. Phys. Chem. A 111, 12584 (2007)
[107] K. P. Puntambekar, P. V. Pesavento, and C. D. Frisbie, Appl. Phys. Lett. 83, 5539 (2003)
[108] K. Seshadri and C. D. Frisbie, Appl. Phys. Lett. 78, 993 (2001)
[109] L. Bürgi, T. J. Richards, R. H. Friend, and H. Sirringhaus, J. Appl. Phys. 94, 6129 (2003)
[110] L. Bürgi, H. Sirringhaus, and R. H. Friend, Appl. Phys. Lett. 80, 2913 (2002)
[111] L. Bürgi, T. Richards, M. Chiesa, R. H. Friend, and H. Sirringhaus, Synth. Met. 146, 297 (2004)
[114] D. Sharma, L. Wang, C. Burham, D. Fine, and A. Dodabalpur, IEDM (2005)
[115] L. Torsi, A. Dodabalapur, L. Sabbatini, and P. G. Zambonin, Sensors and Actuators B 67, 312 (2000)
[116] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger, and Z. Bao, Appl. Phys. Lett. 78, 2229 (2001)
[117] K. Domansky, D. L. Baldwin, J. W. Grate, T. B. Hall, J. Li, M. Josowicz, and J. Janata, Anal. Chem. 70, 473 (1998)
[118] J. Janata and M. Josowicz, Acc. Chem. Res. 31, 241 (1998)
[119] B. H. Hamadani, H. Ding, Y. Gao, and D. Natelson, Phys. Rev. B 72, 235302 (2005)
[120] B. A. Jones, A. Facchetti, M. R. Wasielewski, and T. J. Marks, J. Am. Chem. Soc. 129, 15259 (2007)

Vita

Yeon Taek Jeong was born in Taean-gun, Chungcheongnad-do, The Republic of Korea on June 13, 1971, the son of Jeong Hwa Jeong and Seong Soon Lee. He completed his Bachelor of Science in Materials Engineering from Hanyang University, Seoul, Korea in February 1998. Since then, he worked for Samsung Electronics, Inc. for five and a half years as an engineer in the Liquid Crystal Display (LCD) division. He has been seeking a Ph.D. degree in Materials Science & Engineering from The University of Texas at Austin since fall 2003 under the supervision of Dr. Ananth Dodabalapur, completing the Master of Science in May 2005.

Permanent address: 212 Daegi-ri, Weonbuk-myeon
Taean-gun, Chungcheongnam-do 357-910
The Republic of Korea

This dissertation was typed by the author.